1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

PRODUCTION RELEASED

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
H		468168	PRODUCTION RELEASED	10/17/06	06/22/04

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48	65	HD AND OD FAN	M51_HENRY	08/04/2006
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50	67	TPM	M51_HENRY	08/04/2006
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52	69	AUDIO: LINE INPUT AMP	AUDIO	08/04/2006
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58	75	IMVP6 CPU VCore Regulator	M51_PAUL	08/04/2006
59	76	CPU & SYSTEM SENSE	M51_DAVE	(MASTER)
60	77	PWR GOOD	M51_PAUL	08/04/2006
61	78	3V DC/DC 2.5V	M51_PAUL	08/04/2006
62	79	1.8V & 1.2V VREG	M51_PAUL	08/04/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	08/04/2006
64	82	5V DC/DC	M51_PAUL	08/04/2006
65	83	S0 AND S3 FETS	M51_PAUL	08/04/2006
66	84	MXM PCI-E & PWR	M51_DAVE	(MASTER)
67	85	MXM I/O	M51_DAVE	(MASTER)
68	94	Internal Display Conns	M51_DAVE	(MASTER)
69	97	External Display Conns	M51_DAVE	(MASTER)

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB,SCHEM,MLB,M51	SCH1		
820-1984	1	PCB,FAB,MLB,M51	MLB1		

NEW 630 BOMS AS OF 9/7
CURRENT: REV D 10/17
SCH: REV G

Preliminary

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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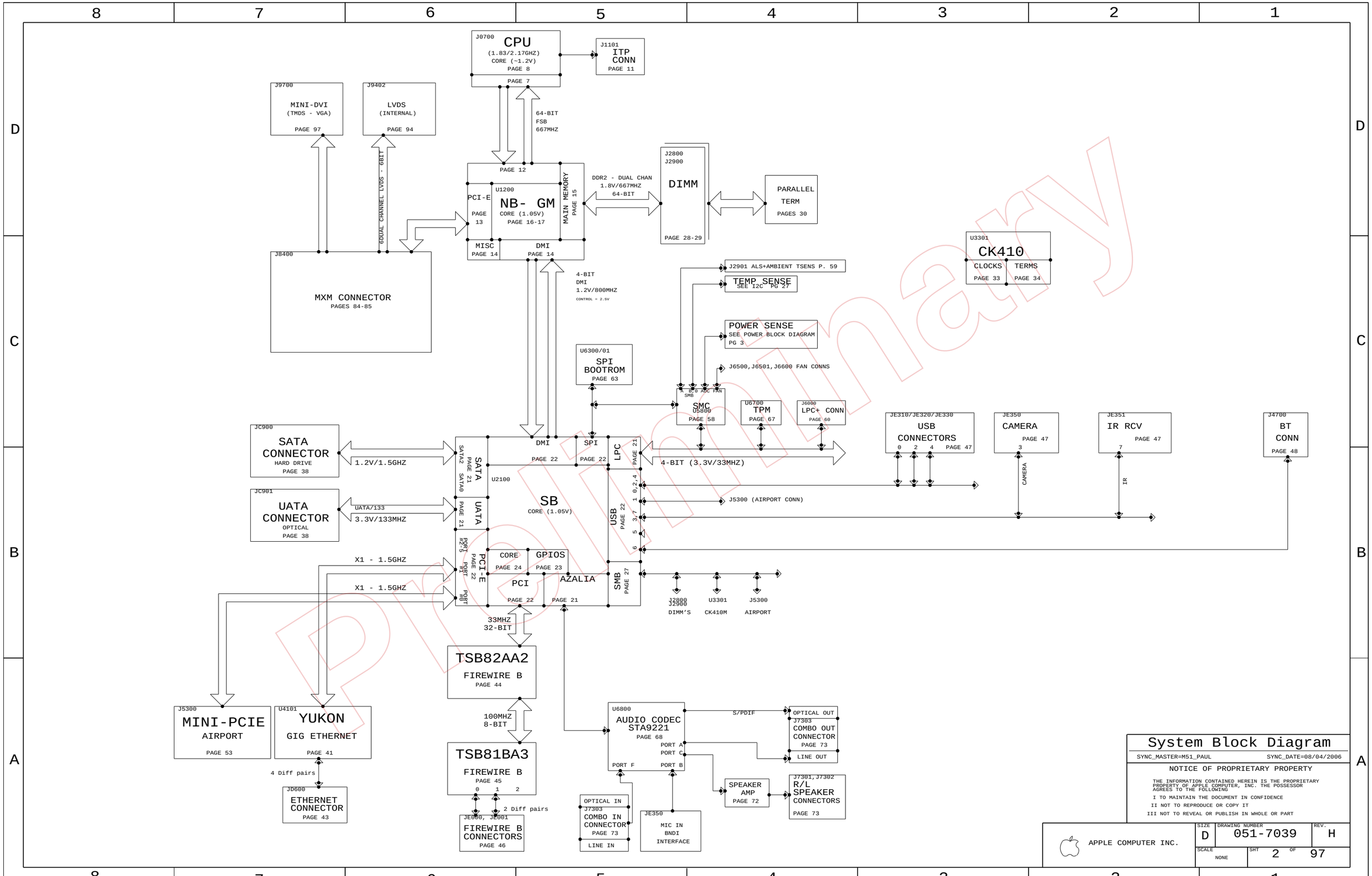
TITLE
SCHEM SANTANA

DRAWING NUMBER 051-7039 REV. H

SHT 1 OF 97



System Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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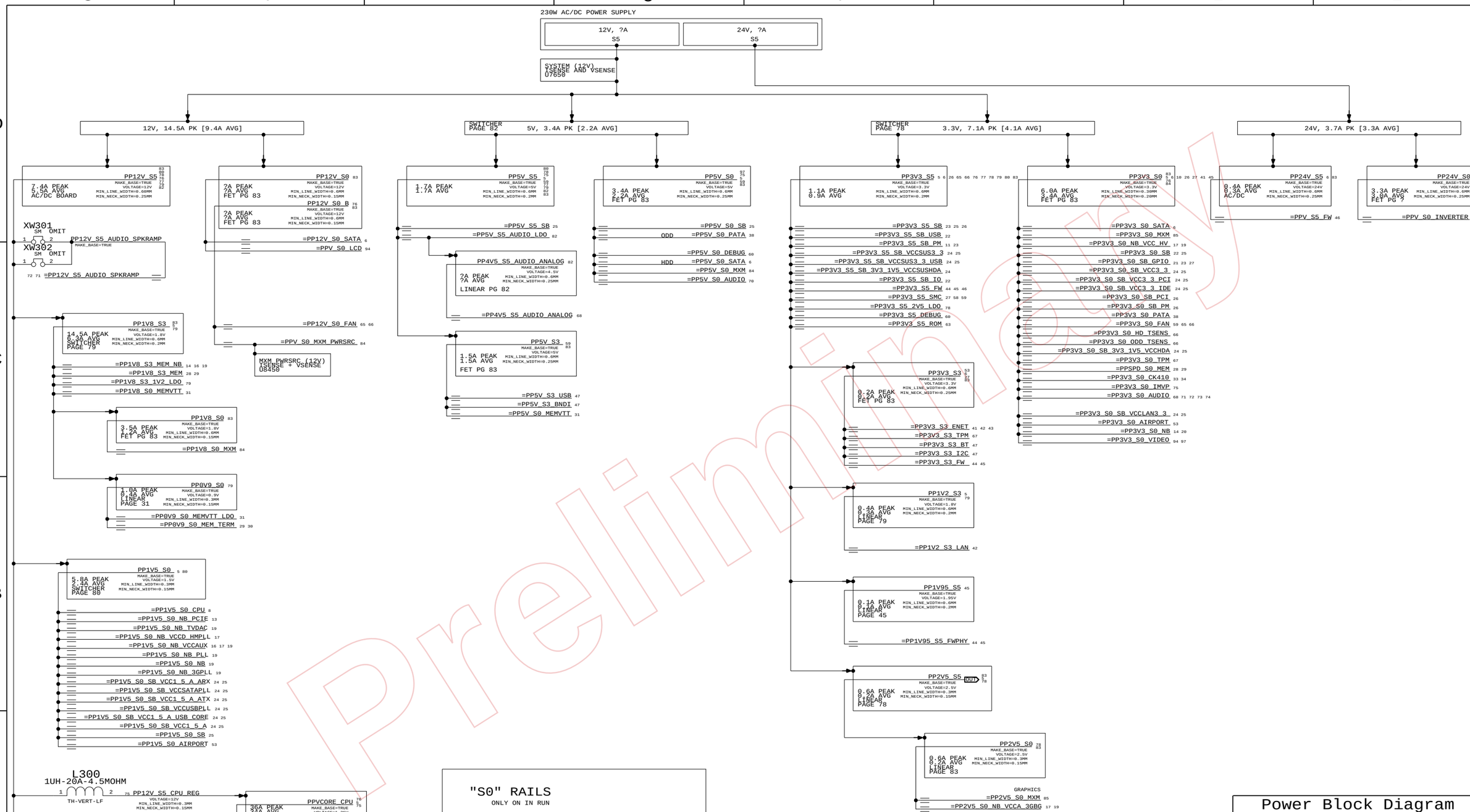
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 2 OF 97	



Preliminary

Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7899	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_WZD,PRODUCTION
630-7898	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_WZC,PRODUCTION

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSENS,CPU_PWR_SENSE
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_TSENS_INT,SYS_PWR_SENSE,MXM_PWR_SENSE

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

BarCode Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:WZD]	CRITICAL	EEE_WZD
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:WZC]	CRITICAL	EEE_WZC

CHIPSET, ROMS, ETC.

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
	511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
	338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
	343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
	359S0117	1	IC,SLG84435,CLK GEN,68PIN QFN	U3301	CRITICAL	
	338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
	341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
	353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
	341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM
(335S0384)	341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	
(338S0274)	341T0020	1	IC,SMC,M51	U5800	CRITICAL	

PROCESSORS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3392	1	MEROM 2.33GHZ, M51	CPU	CRITICAL	M51_BEST
337S3390	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	

BATTERY IS INSTALLED AT FATP

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.
124-0361	124-0339		ALL	SANYO ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
353S1461	353S1465		U7500	CPU VREG NEW REV
740S0044	740S0028		F9710	DVI DDC (LITTLEFUSE)
138S0567	138S0516		ALL	CAP CONSOLIDATION
376S0388	376S0444		ALL	ON SEMI 2ND SRC FOR IR

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8458	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C8459	PRODUCTION

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K-OHM,5%,0402	C7602	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C7612	NOSTUFF

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

Preliminary

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H

SCALE NONE SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 OMIT P4MM

34 22 PCI_CLK_SB PP6D0 OMIT P4MM
44 34 PCI_CLK_FW PP626 OMIT P4MM
58 34 PCI_CLK_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 OMIT P4MM
38 21 IDE_PDIORDY PP6C7 OMIT P4MM
38 21 IDE_PDD<9> PP6C8 OMIT P4MM

54 22 PCIE_B_D2R_P PP600 OMIT P4MM
54 22 PCIE_B_D2R_N PP601 OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 OMIT P4MM
63 58 22 SPI_SO PP612 OMIT P4MM
63 58 22 SPI_SI PP613 OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 OMIT P4MM
27 SMBUS_SB_SDA PP605 OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 OMIT P4MM

FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 OMIT P4MM
14 NB_RST_IN_L_R PP666 OMIT P4MM

22 14 DMI_S2N_N<0> PP673 OMIT P4MM
22 14 DMI_S2N_P<0> PP674 OMIT P4MM

19 14 MEM_VREF_NB_0 PP6E1 OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 OMIT P4MM

14 NB_CFG<17>	I473	NC_NB_CFG<17>	MAKE_BASE=TRUE
14 NB_CFG<15>	I474	NC_NB_CFG<15>	MAKE_BASE=TRUE
14 NB_CFG<14>	I475	NC_NB_CFG<14>	MAKE_BASE=TRUE
14 NB_CFG<13>	I476	NC_NB_CFG<13>	MAKE_BASE=TRUE
14 NB_CFG<12>	I477	NC_NB_CFG<12>	MAKE_BASE=TRUE
14 NB_CFG<11>	I478	NC_NB_CFG<11>	MAKE_BASE=TRUE
14 NB_CFG<10>	I479	NC_NB_CFG<10>	MAKE_BASE=TRUE
14 NB_CFG<8>	I481	NC_NB_CFG<8>	MAKE_BASE=TRUE
14 NB_CFG<6>	I480	NC_NB_CFG<6>	MAKE_BASE=TRUE
14 NB_CFG<4>	I482	NC_NB_CFG<4>	MAKE_BASE=TRUE
14 NB_CFG<3>	I483	NC_NB_CFG<3>	MAKE_BASE=TRUE

22 PCI_GNT3_L I513 TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT

22 USB_F_N TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL

19 13 LVDS_BKLTEN TP_LVDS_BKLTEN MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN	PEG_R2D_C_N<0>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<0>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<1>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<1>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<2>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<2>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<3>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<3>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<4>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<4>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<5>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<5>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<6>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<6>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<7>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<7>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<8>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<8>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<9>	NO_TEST=TRUE
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84 13 IN	PEG_R2D_C_N<10>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<10>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<11>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<11>	NO_TEST=TRUE
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84 13 IN	PEG_R2D_C_N<14>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<14>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_N<15>	NO_TEST=TRUE
84 13 IN	PEG_R2D_C_P<15>	NO_TEST=TRUE

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84 IN	PEG_R2D_P<1>	NO_TEST=TRUE
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84 IN	PEG_R2D_P<2>	NO_TEST=TRUE
84 IN	PEG_R2D_N<3>	NO_TEST=TRUE
84 IN	PEG_R2D_P<3>	NO_TEST=TRUE
84 IN	PEG_R2D_N<4>	NO_TEST=TRUE
84 IN	PEG_R2D_P<4>	NO_TEST=TRUE
84 IN	PEG_R2D_N<5>	NO_TEST=TRUE
84 IN	PEG_R2D_P<5>	NO_TEST=TRUE
84 IN	PEG_R2D_N<6>	NO_TEST=TRUE
84 IN	PEG_R2D_P<6>	NO_TEST=TRUE
84 IN	PEG_R2D_N<7>	NO_TEST=TRUE
84 IN	PEG_R2D_P<7>	NO_TEST=TRUE
84 IN	PEG_R2D_N<8>	NO_TEST=TRUE
84 IN	PEG_R2D_P<8>	NO_TEST=TRUE
84 IN	PEG_R2D_N<9>	NO_TEST=TRUE
84 IN	PEG_R2D_P<9>	NO_TEST=TRUE
84 IN	PEG_R2D_N<10>	NO_TEST=TRUE
84 IN	PEG_R2D_P<10>	NO_TEST=TRUE
84 IN	PEG_R2D_N<11>	NO_TEST=TRUE
84 IN	PEG_R2D_P<11>	NO_TEST=TRUE
84 IN	PEG_R2D_N<12>	NO_TEST=TRUE
84 IN	PEG_R2D_P<12>	NO_TEST=TRUE
84 IN	PEG_R2D_N<13>	NO_TEST=TRUE
84 IN	PEG_R2D_P<13>	NO_TEST=TRUE
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84 IN	PEG_R2D_P<14>	NO_TEST=TRUE
84 IN	PEG_R2D_N<15>	NO_TEST=TRUE
84 IN	PEG_R2D_P<15>	NO_TEST=TRUE

84 13 IN	PEG_D2R_N<0>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<0>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<1>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<1>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<2>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<2>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<3>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<3>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<4>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<4>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<5>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<5>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<6>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<6>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<7>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<7>	NO_TEST=TRUE
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84 13 IN	PEG_D2R_P<8>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<9>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<9>	NO_TEST=TRUE
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84 13 IN	PEG_D2R_N<11>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<11>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<12>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<12>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<13>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<13>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<14>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<14>	NO_TEST=TRUE
84 13 IN	PEG_D2R_N<15>	NO_TEST=TRUE
84 13 IN	PEG_D2R_P<15>	NO_TEST=TRUE

76 75 3 IN	PPVCORE_CPU	FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 83 IN	PP3V3_S5	FUNC_TEST=TRUE
83 78 3 IN	PP2V5_S5	FUNC_TEST=TRUE
83 79 3 IN	PP1V8_S3	FUNC_TEST=TRUE
79 3 IN	PP1V2_S3	FUNC_TEST=TRUE
80 3 IN	PP1V5_S0	FUNC_TEST=TRUE
80 34 3 IN	PP1V05_S0	FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN	PP5V_S5	FUNC_TEST=TRUE
97 83 75 59 3 IN	PP5V_S0	FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN	PP5V_S5	FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 83 IN	PP3V3_S5	FUNC_TEST=TRUE
84 83 76 45 41 27 26 10 6 3 IN	PP3V3_S0	FUNC_TEST=TRUE
83 3 IN	PP24V_S0	FUNC_TEST=TRUE

11 7 IN	XDP_BPM_L<3>	FUNC_TEST=TRUE
11 7 IN	XDP_BPM_L<2>	FUNC_TEST=TRUE
11 7 IN	XDP_BPM_L<1>	FUNC_TEST=TRUE
11 7 IN	XDP_BPM_L<0>	FUNC_TEST=TRUE
26 11 7 IN	XDP_DBRESET_L	FUNC_TEST=TRUE
26 5 IN	SW_RST_BTN_L	FUNC_TEST=TRUE
59 5 IN	POWER_BUTTON_L	FUNC_TEST=TRUE
67 60 58 21 IN	LPC_AD<0>	FUNC_TEST=TRUE
67 60 58 21 IN	LPC_AD<1>	FUNC_TEST=TRUE
67 60 58 21 IN	LPC_AD<2>	FUNC_TEST=TRUE
67 60 58 21 IN	LPC_AD<3>	FUNC_TEST=TRUE
67 60 58 21 5 IN	LPC_FRAME_L	FUNC_TEST=TRUE
67 60 58 23 IN	PM_CLKRUN_L	FUNC_TEST=TRUE
60 58 22 IN	BOOT_LPC_SPI_L	FUNC_TEST=TRUE
60 6 IN	DEBUG_RST_L	FUNC_TEST=TRUE
60 59 21 IN	FWH_INIT_L	FUNC_TEST=TRUE
60 34 IN	PCI_CLK_PORT80	FUNC_TEST=TRUE
67 60 58 23 IN	INT_SERIRQ	FUNC_TEST=TRUE
67 60 58 23 IN	PM_SUS_STAT_L	FUNC_TEST=TRUE
60 58 IN	SMC_MD1	FUNC_TEST=TRUE
60 59 58 IN	SMC_RST_L	FUNC_TEST=TRUE
60 58 IN	SMC_NMI	FUNC_TEST=TRUE
60 23 IN	SV_SET_UP	FUNC_TEST=TRUE
76 58 IN	ISENSE_CAL_EN	FUNC_TEST=TRUE
94 85 IN	INV_ENABLE_BL	FUNC_TEST=TRUE
94 IN	LCD_PWM	FUNC_TEST=TRUE
75 8 IN	CPU_VID<0>	FUNC_TEST=TRUE
75 8 IN	CPU_VID<1>	FUNC_TEST=TRUE
75 8 IN	CPU_VID<2>	FUNC_TEST=TRUE
75 8 IN	CPU_VID<3>	FUNC_TEST=TRUE
75 8 IN	CPU_VID<4>	FUNC_TEST=TRUE
75 8 IN	CPU_VID<5>	FUNC_TEST=TRUE
75 8 IN	CPU_VID<6>	FUNC_TEST=TRUE
75 23 14 IN	PM_DPRSLPVR	FUNC_TEST=TRUE
75 21 7 IN	CPU_DPRSTP_L	FUNC_TEST=TRUE
75 26 14 5 IN	VR_PWRGOOD_DELAY	FUNC_TEST=TRUE
26 23 IN	VR_PWRGD_CK410	FUNC_TEST=TRUE
84 77 58 26 IN	ALL_SYS_PWRGD	FUNC_TEST=TRUE
77 58 23 IN	PM_SLP_S4_L	FUNC_TEST=TRUE
80 79 77 58 23 IN	PM_SLP_S3_L	FUNC_TEST=TRUE

60 59 58 IN	SMC_TCK	FUNC_TEST=TRUE
60 59 58 IN	SMC_TDI	FUNC_TEST=TRUE
60 59 58 IN	SMC_TDO	FUNC_TEST=TRUE
60 59 58 IN	SMC_TMS	FUNC_TEST=TRUE
60 58 IN	SMC_TRST_L	FUNC_TEST=TRUE
60 59 58 IN	SMC_TX_L	FUNC_TEST=TRUE
60 59 58 IN	SMC_RX_L	FUNC_TEST=TRUE
59 IN	SMC_MANUAL_RST_L	FUNC_TEST=TRUE
11 7 IN	XDP_TCK	FUNC_TEST=TRUE
11 7 IN	XDP_TDI	FUNC_TEST=TRUE
11 7 IN	XDP_TDO	FUNC_TEST=TRUE
11 7 IN	XDP_TMS	FUNC_TEST=TRUE
11 7 IN	XDP_TRST_L	FUNC_TEST=TRUE
59 5 IN	POWER_BUTTON_L	FUNC_TEST=TRUE
26 5 IN	SW_RST_BTN_L	FUNC_TEST=TRUE
10 IN	NB_TSENS_HS_DXP	FUNC_TEST=TRUE
10 IN	NB_TSENS_HS_DXN	FUNC_TEST=TRUE
34 11 IN	CPU_XDP_CLK_N	FUNC_TEST=TRUE
34 11 IN	CPU_XDP_CLK_P	FUNC_TEST=TRUE
11 IN	ITPRESET_L	FUNC_TEST=TRUE
11 7 IN	XDP_BPM_L<5>	FUNC_TEST=TRUE
11 7 IN	XDP_BPM_L<4>	FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA
ZH510 HOLE-VIA
ZH520 HOLE-VIA
ZH501 HOLE-VIA
ZH511 HOLE-VIA
ZH521 HOLE-VIA
ZH502 HOLE-VIA
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ZH528 HOLE-VIA
ZH509 HOLE-VIA
ZH519 HOLE-VIA
ZH529 HOLE-VIA

FUNC TEST 1 OF 2

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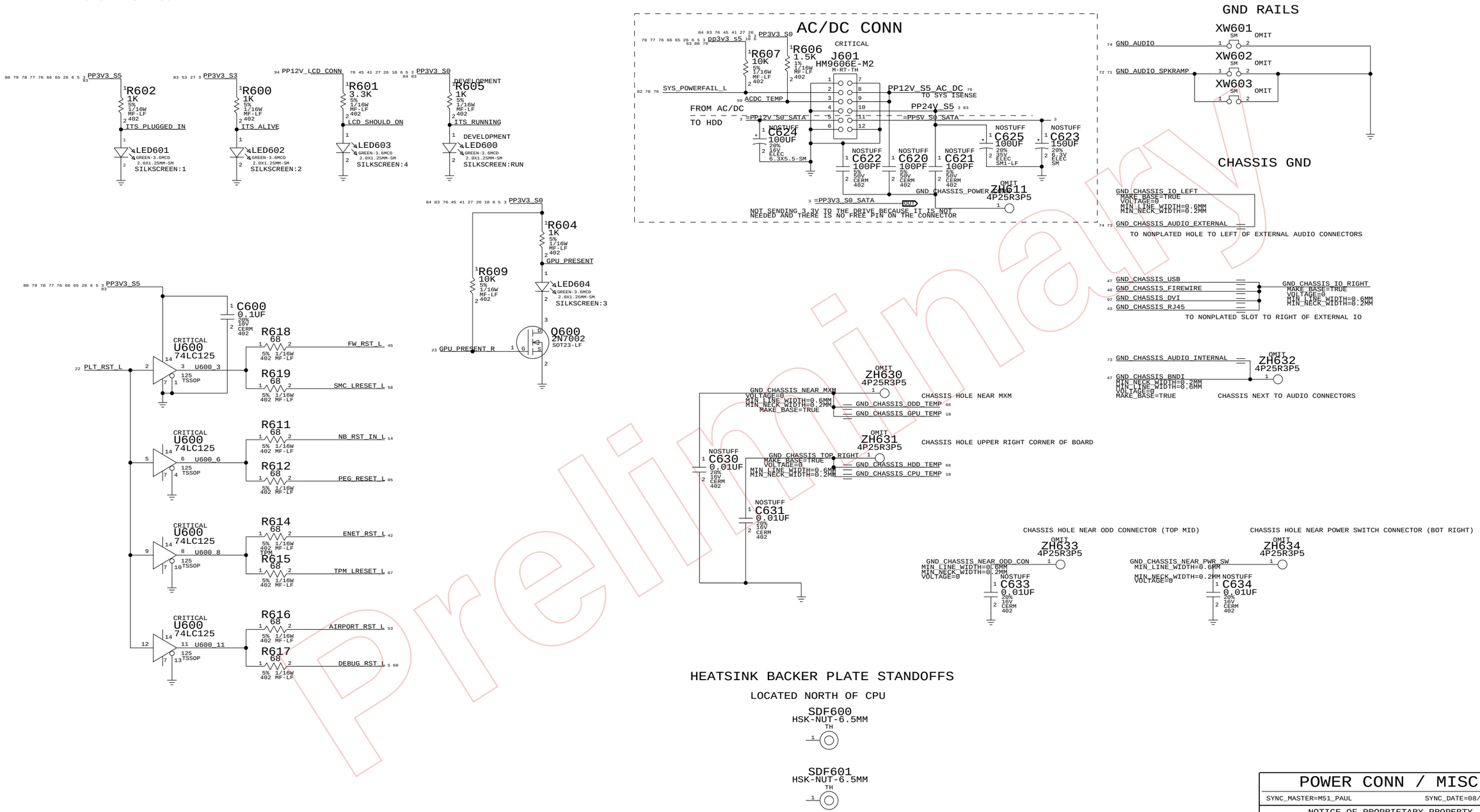

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POWER CONN / MISC

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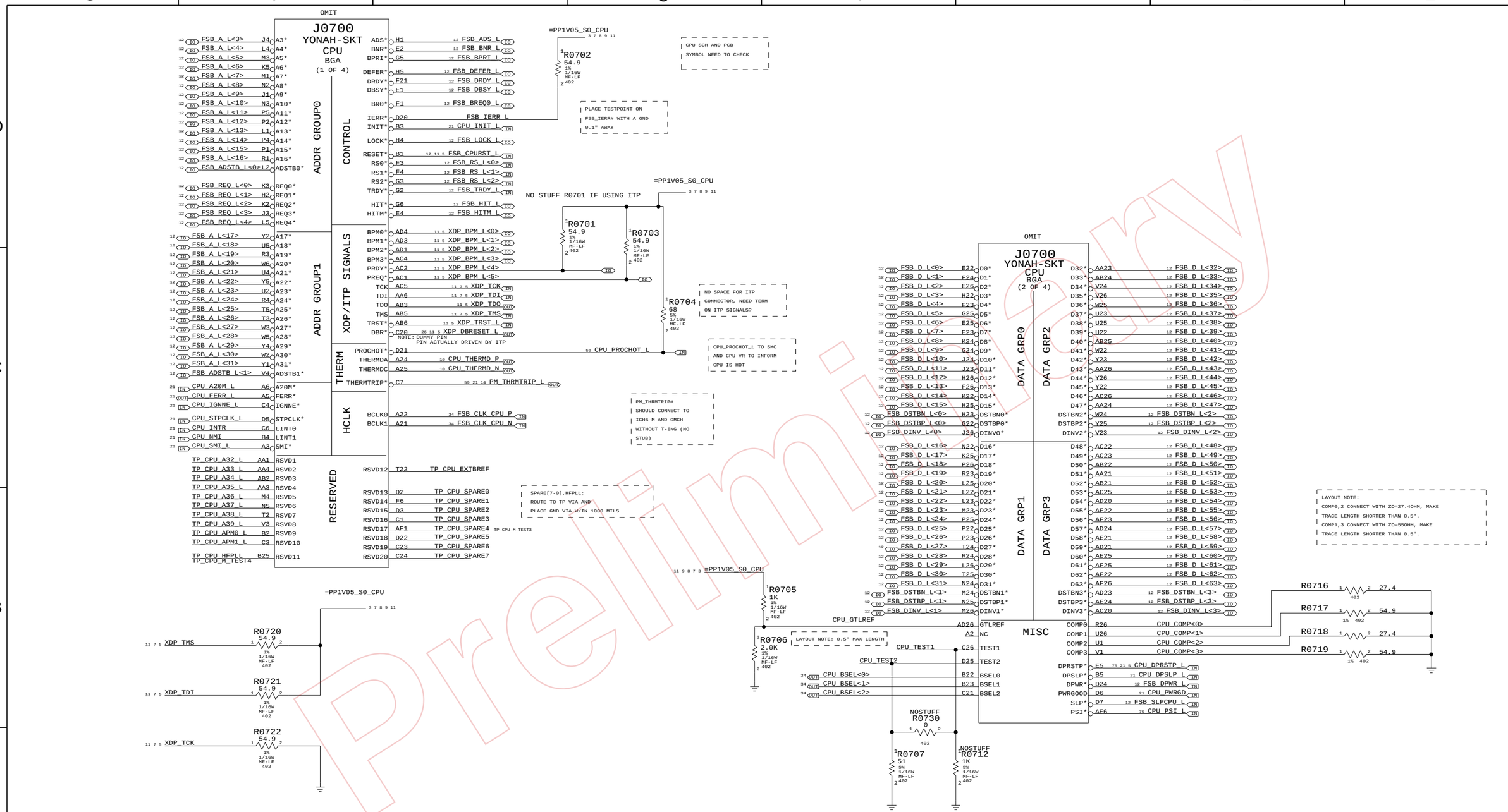

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CPU 1 OF 2-FSB

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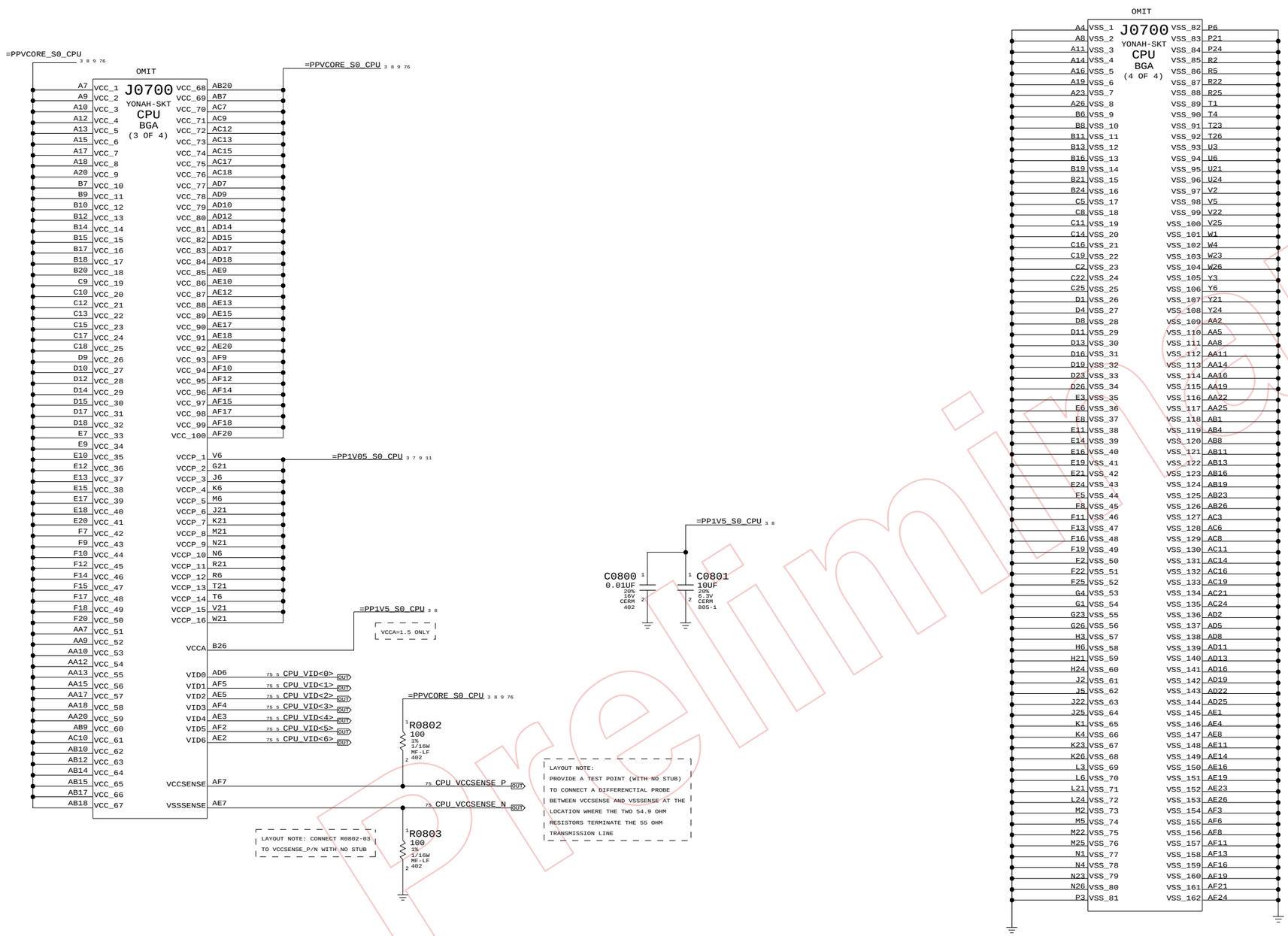

CPU 2 OF 2-PWR/GND

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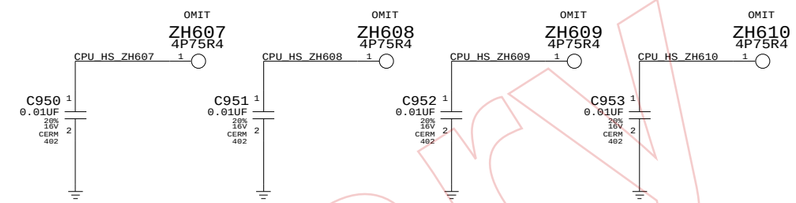
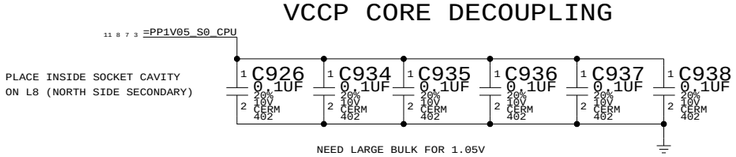
CPU HEATSINK MOUNTING HOLES

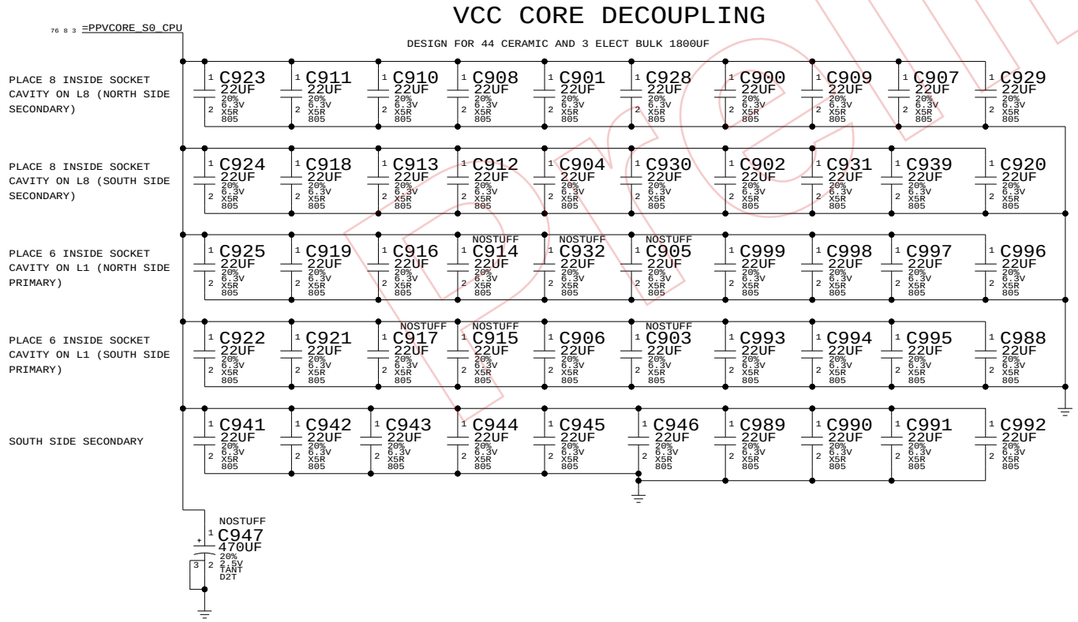


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING



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CPU DECAPS & VID<>

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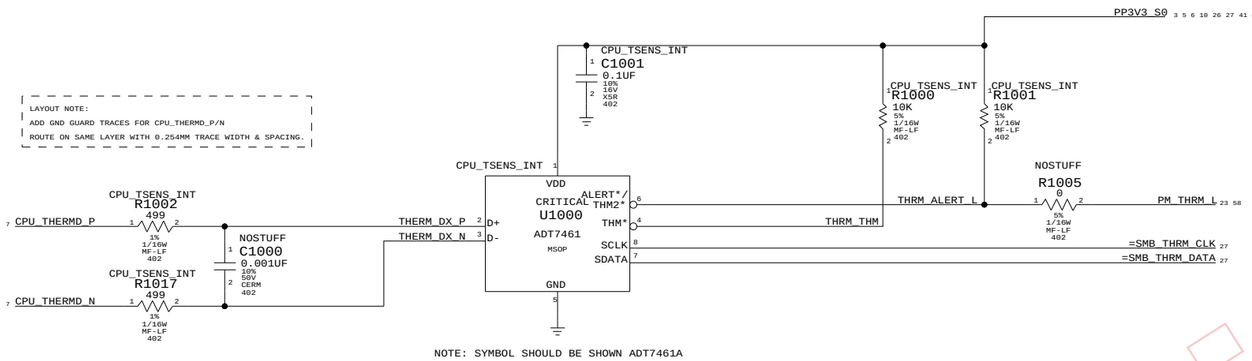
CPU INTERNAL DIODE THERMAL SENSOR

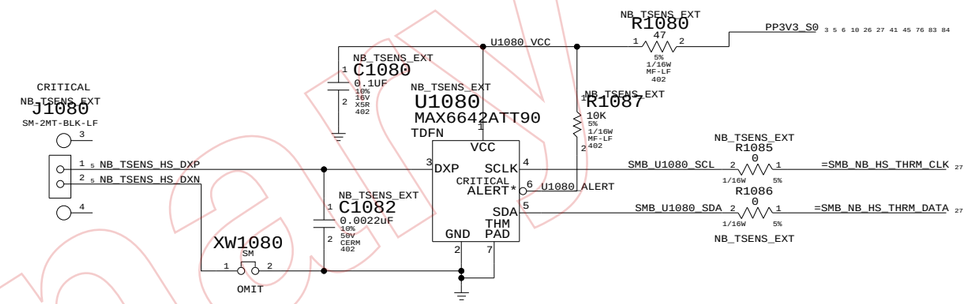
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



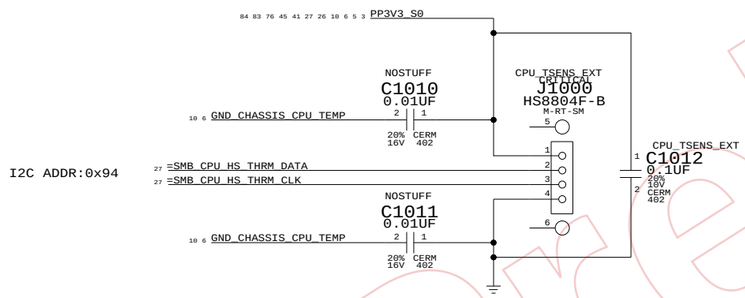
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

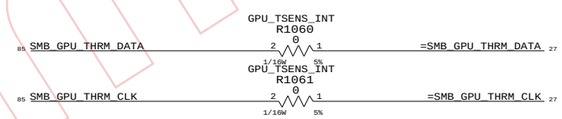


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

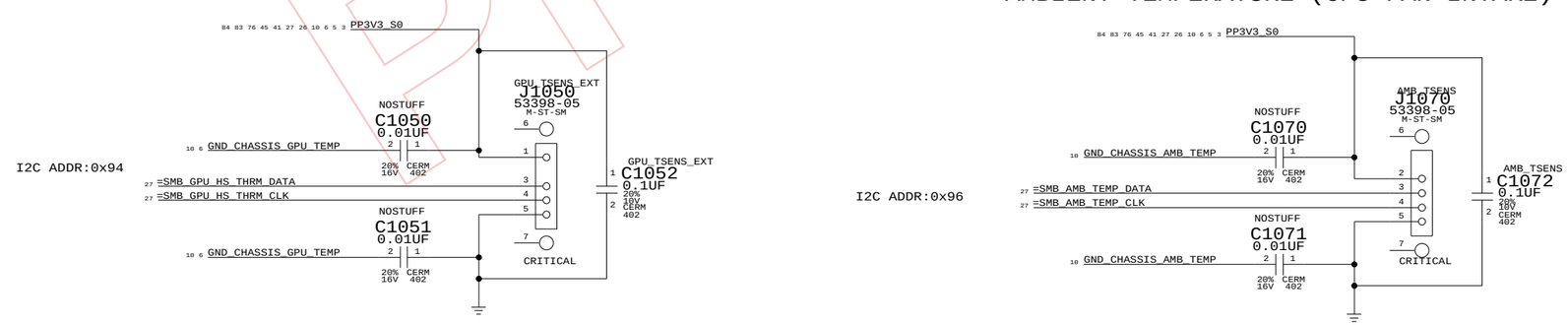


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



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ASIC TEMP SENSORS

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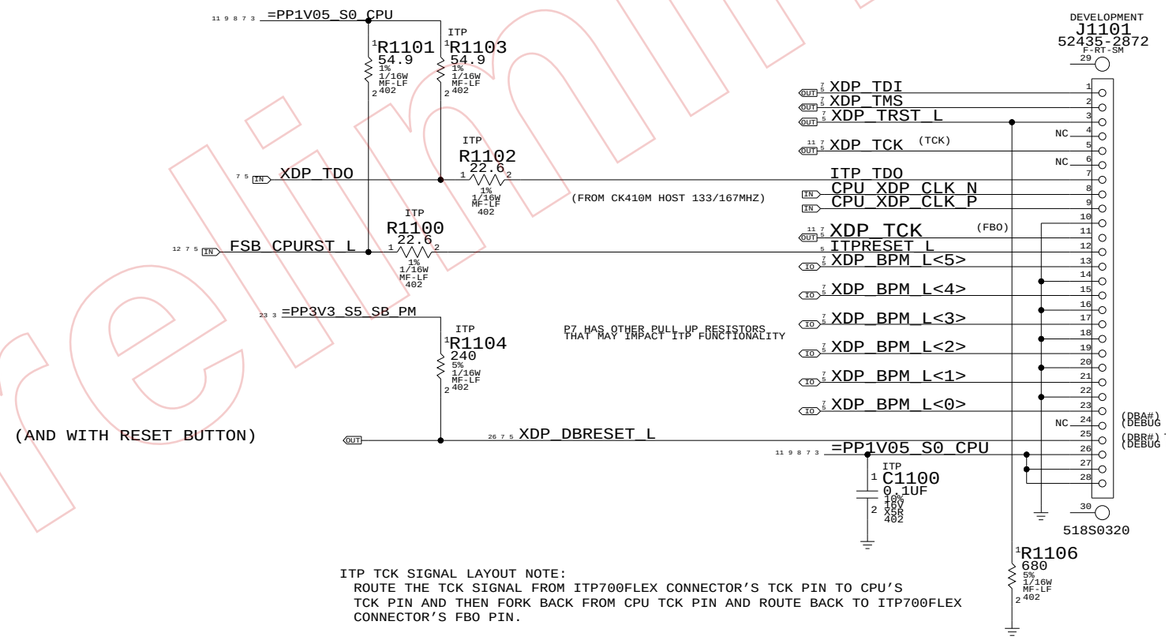
CPU ITP700FLEX DEBUG SUPPORT



(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

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CPU ITP700FLEX DEBUG

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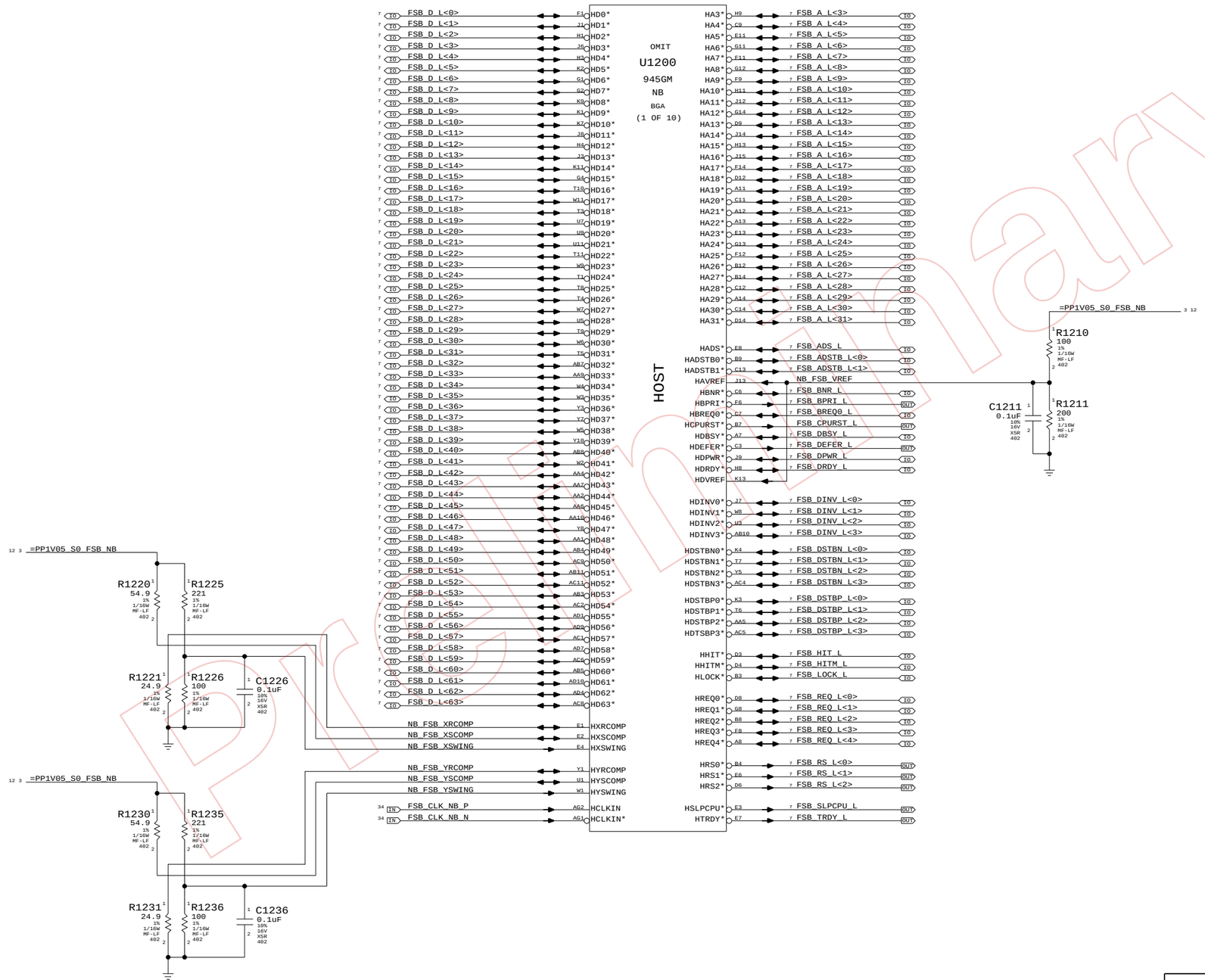

NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

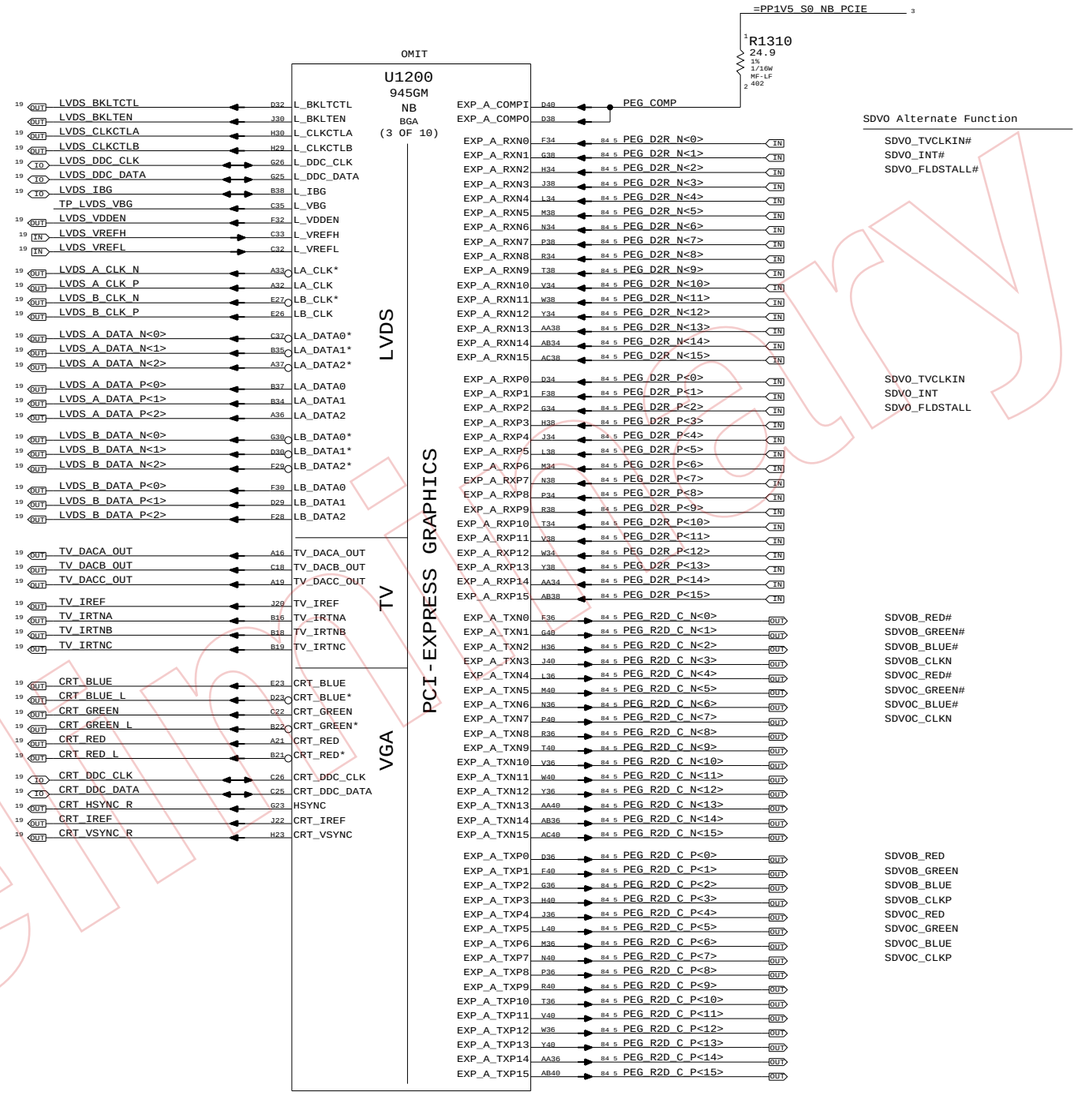
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



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NB PEG / Video Interfaces

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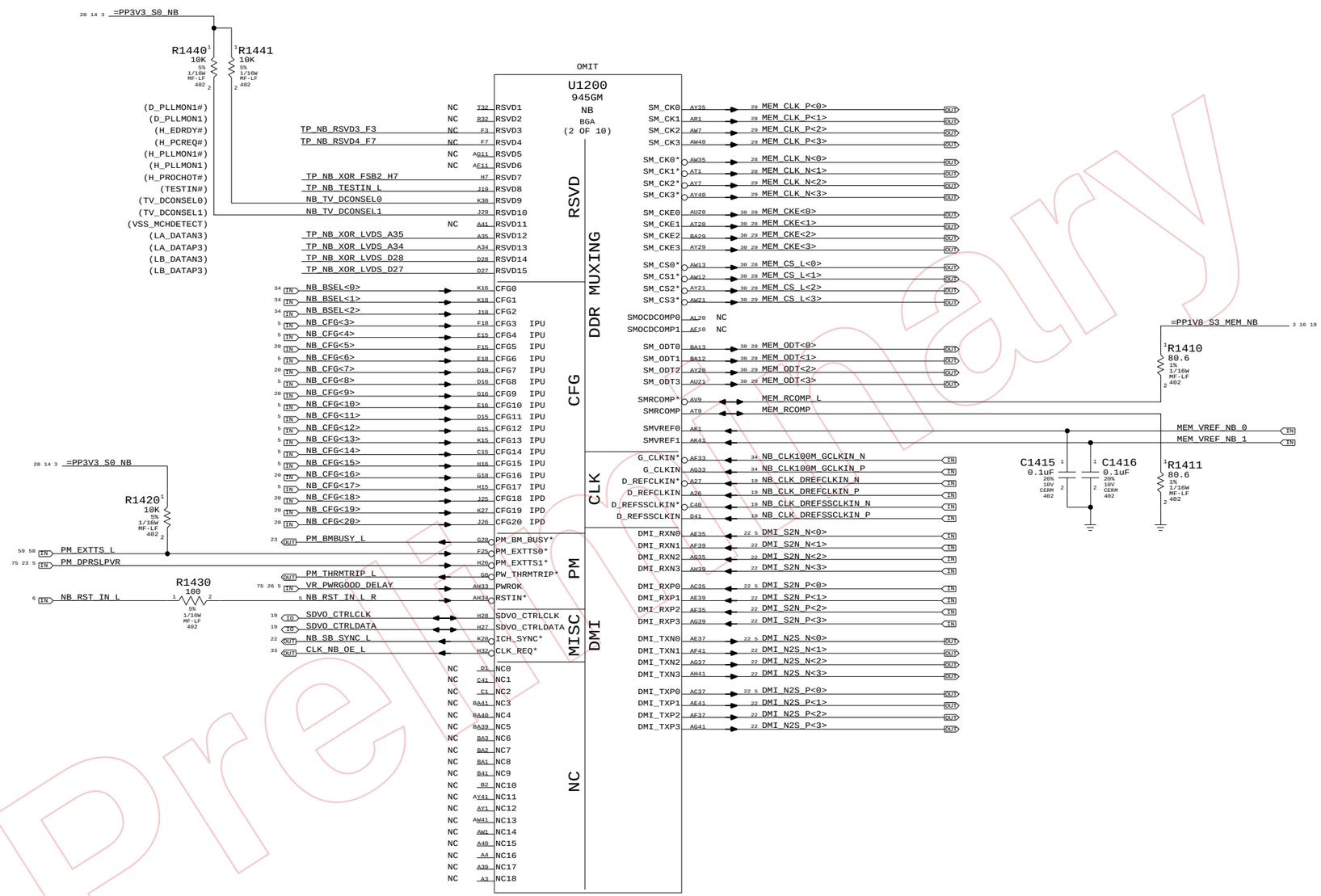

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NB Misc Interfaces

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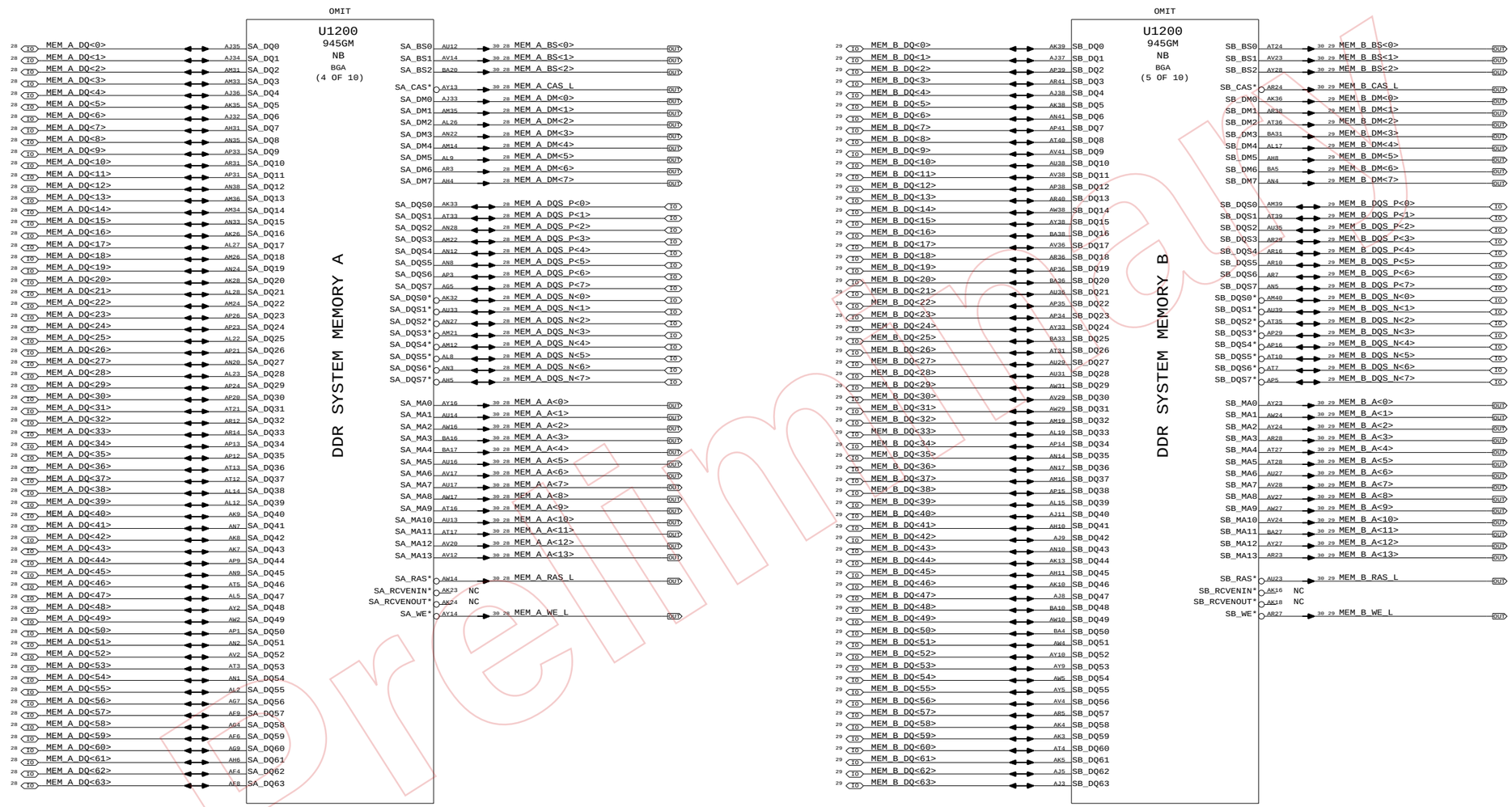

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NB DDR2 Interfaces

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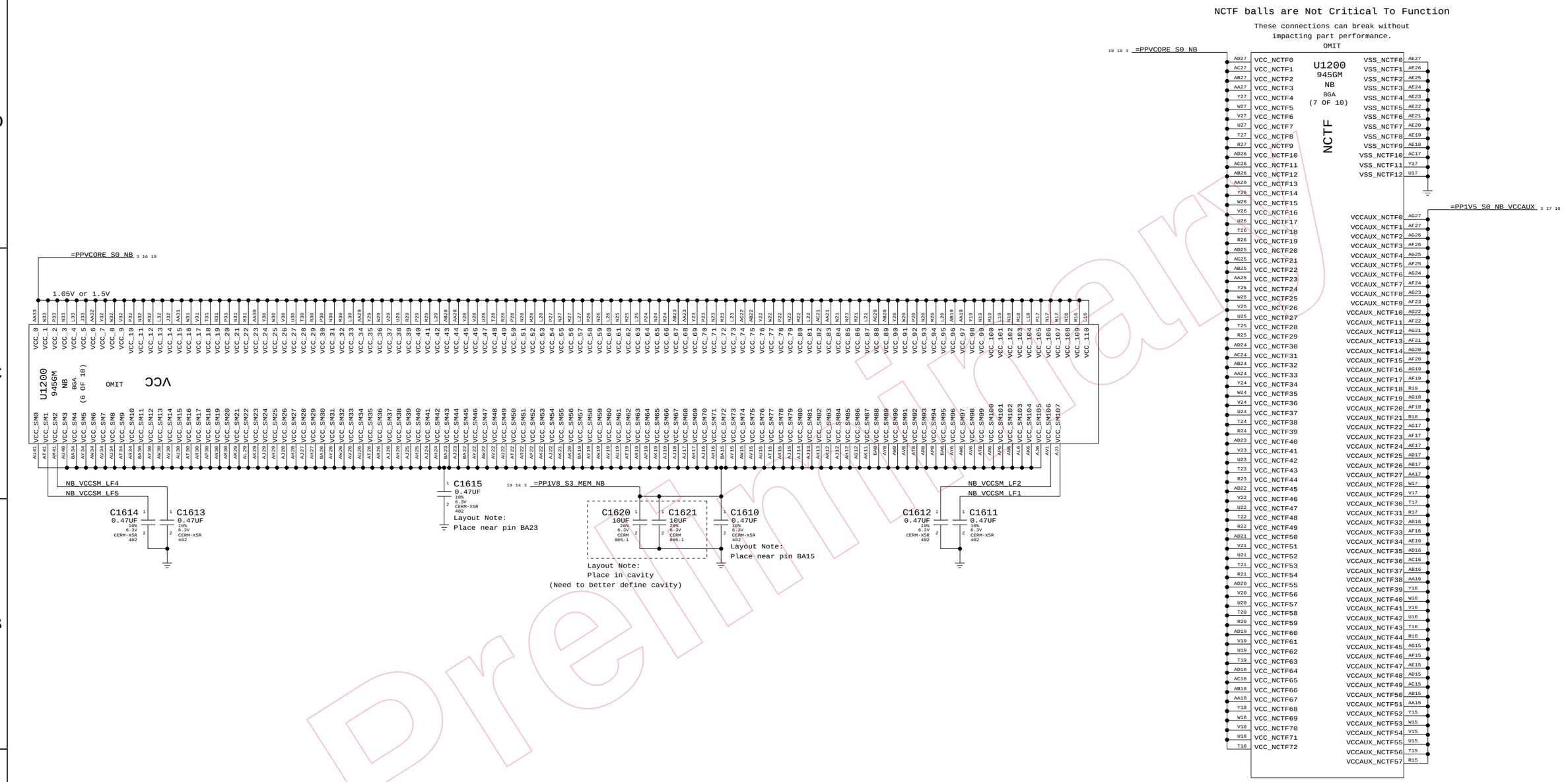

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NB Power 1

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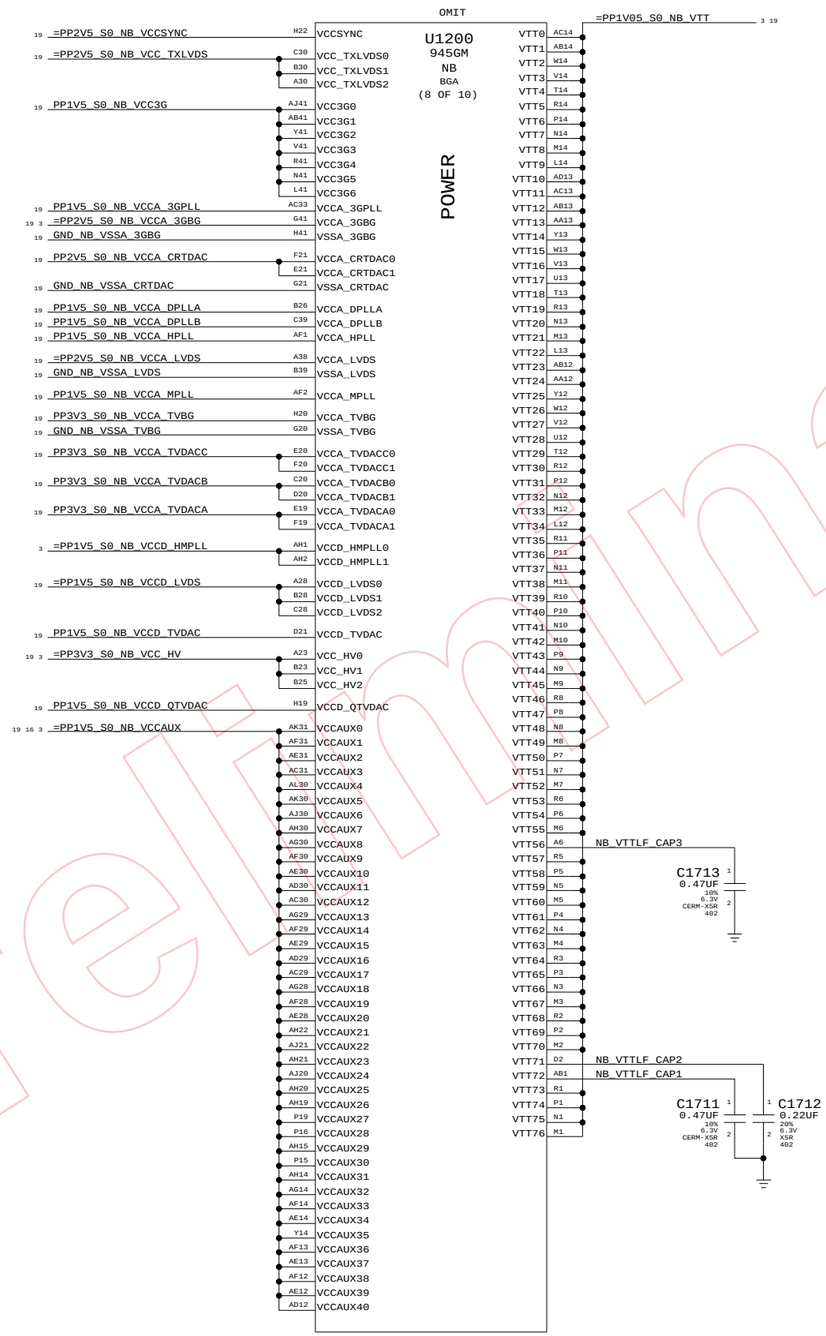

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NB Power 2

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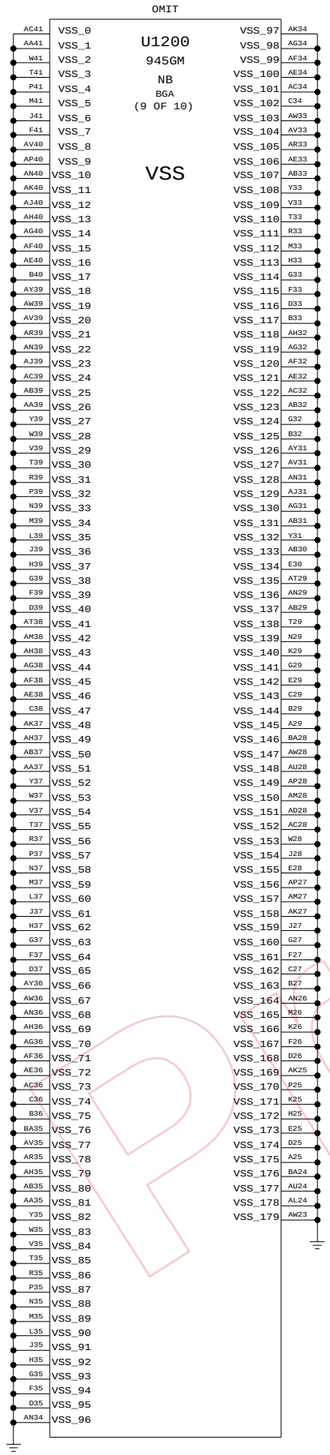

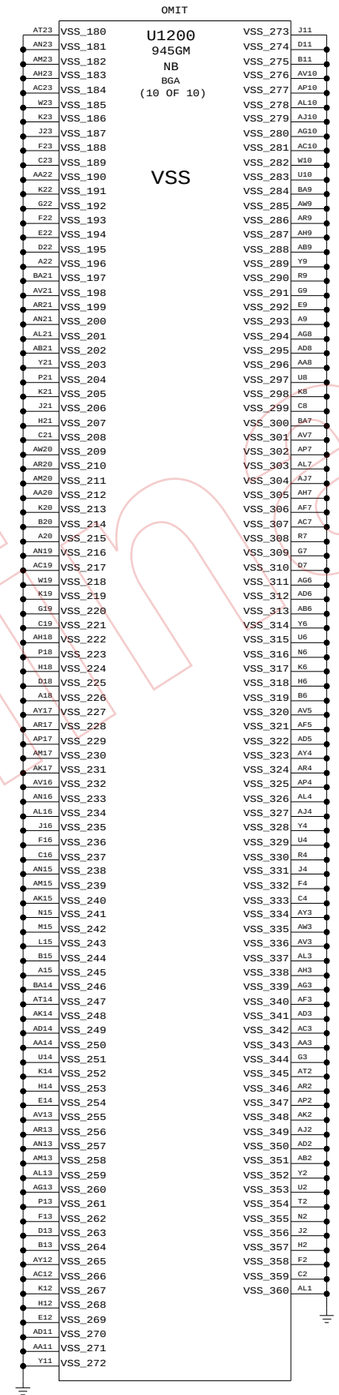

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NB Grounds

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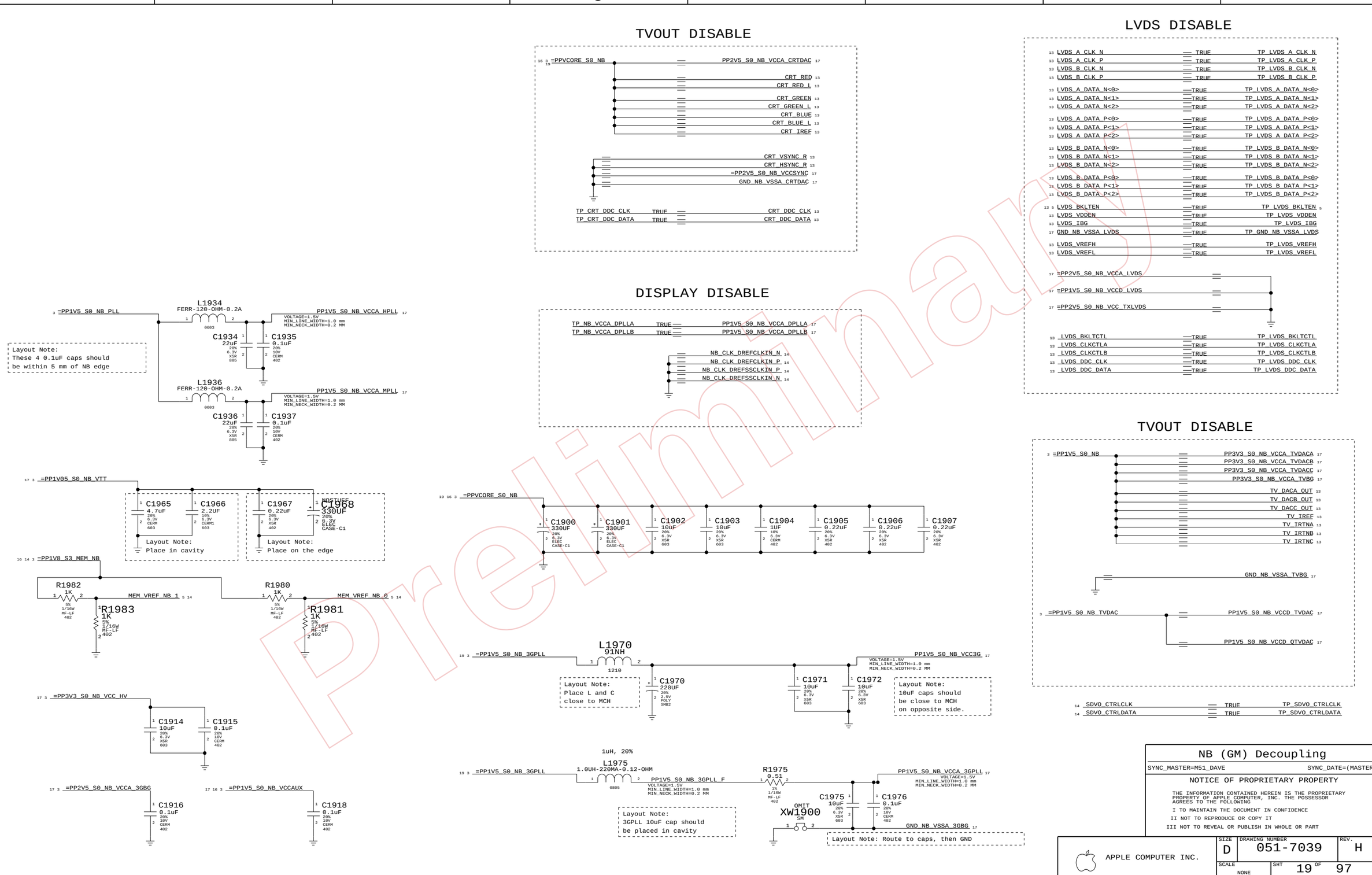

NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 19 OF 97	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

Preliminary

NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=08/04/2006

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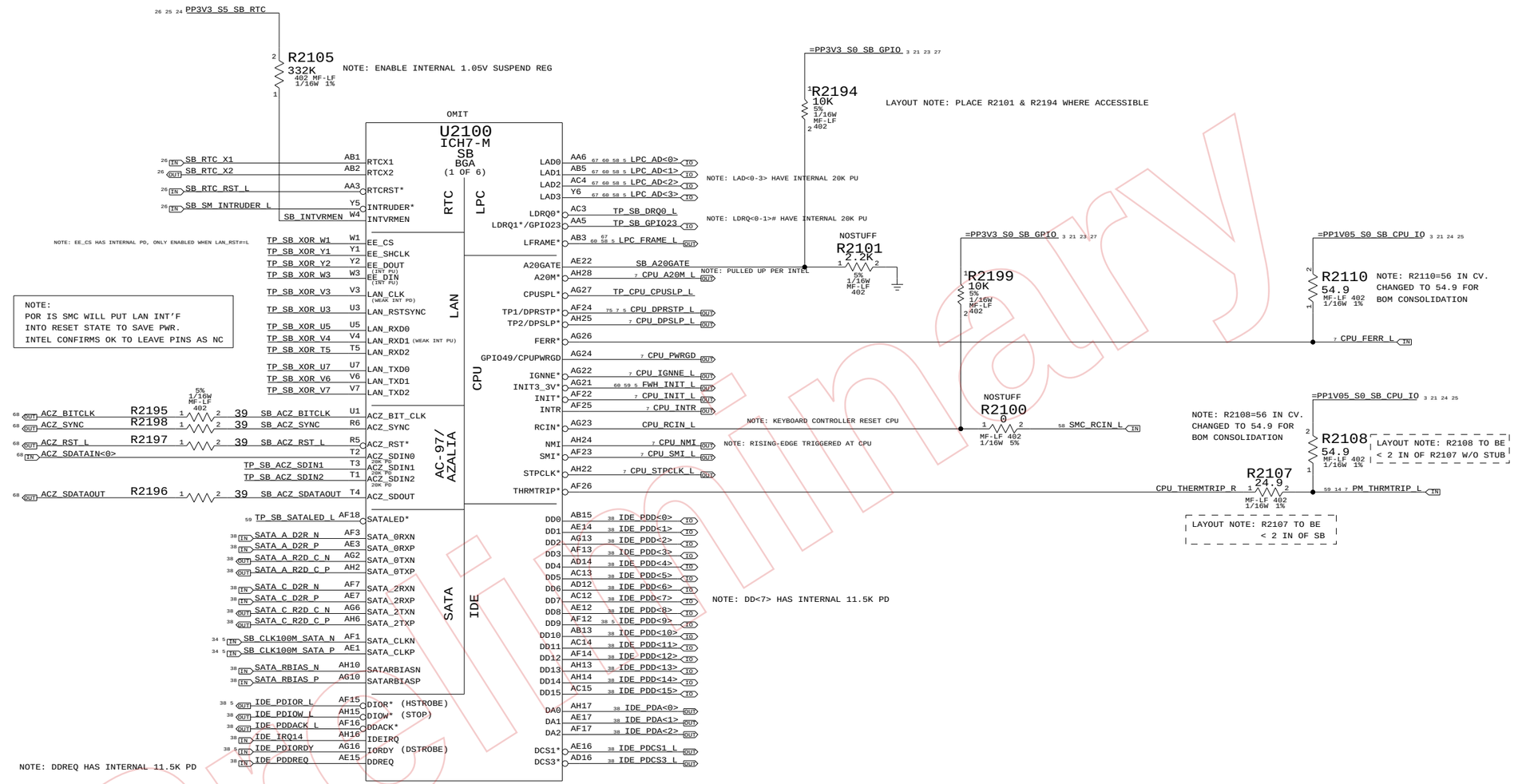
SCALE NONE	SHT 20 OF 97	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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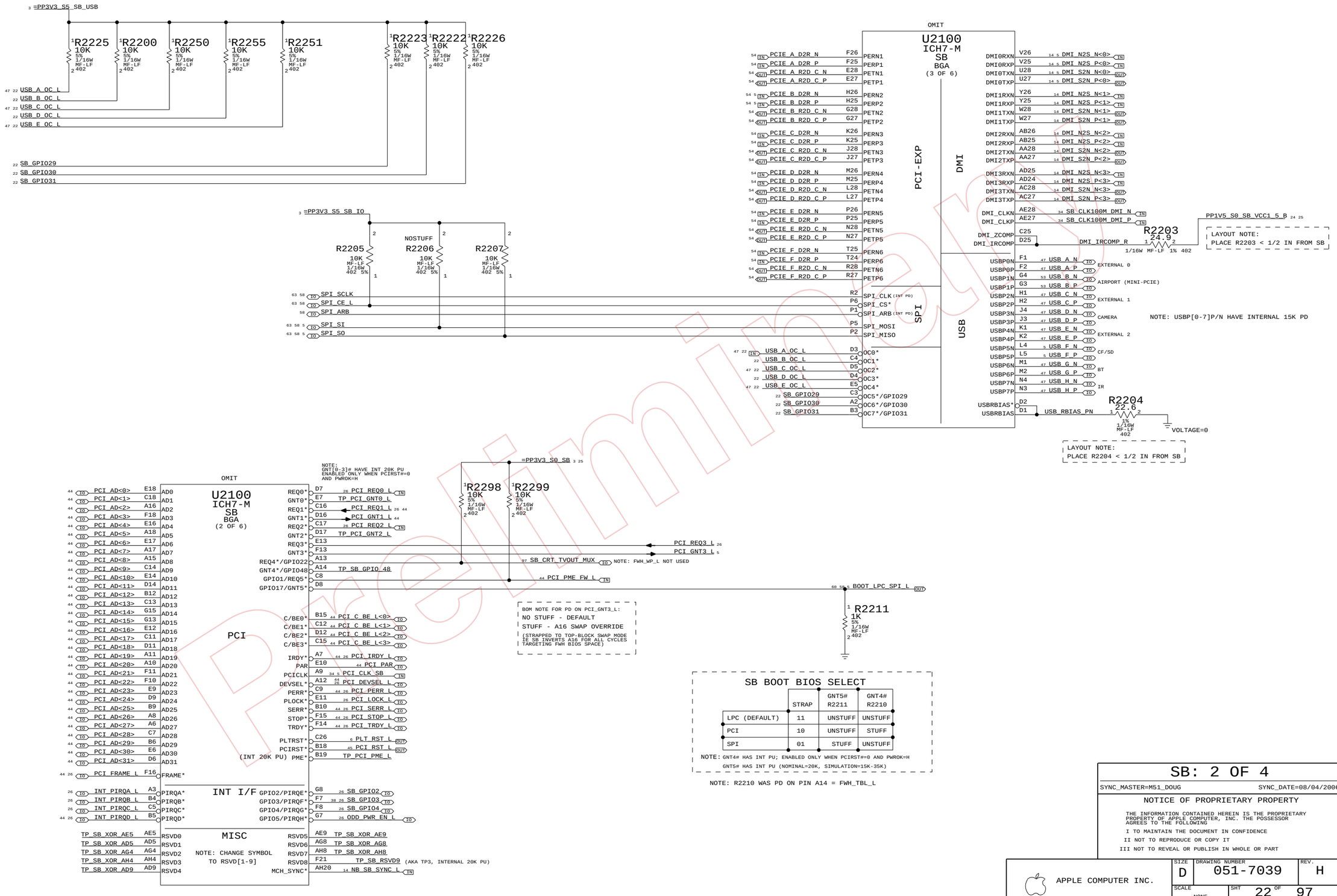
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 21 OF 97	

Preliminary



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SB: 2 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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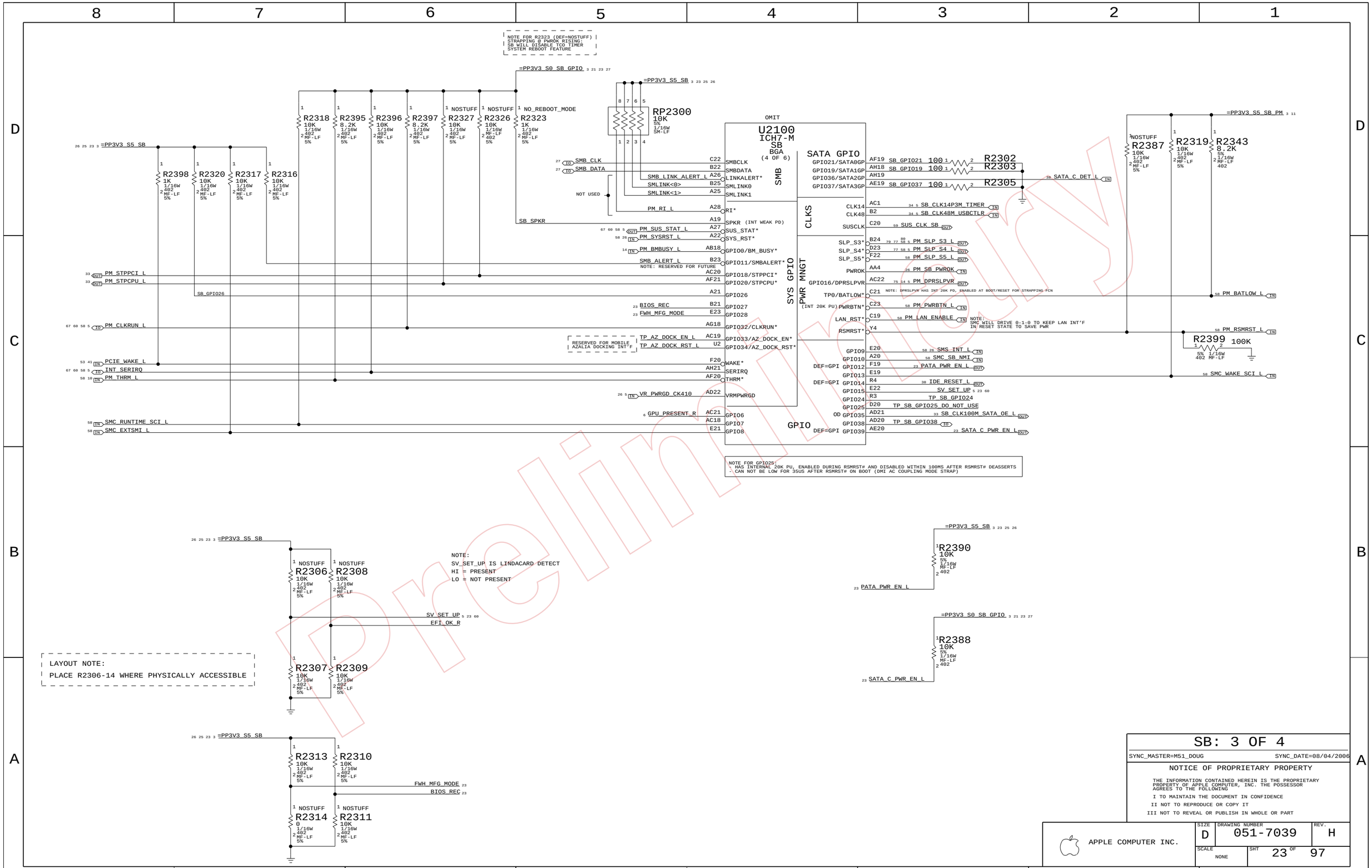
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 22 OF 97	



SB: 3 OF 4	
SYNC_MASTER=M51_DOUG	SYNC_DATE=08/04/2006

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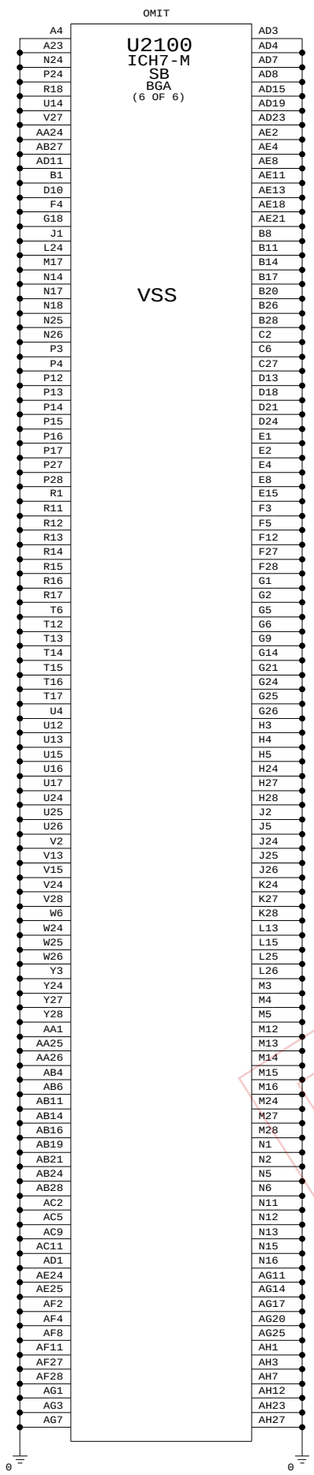
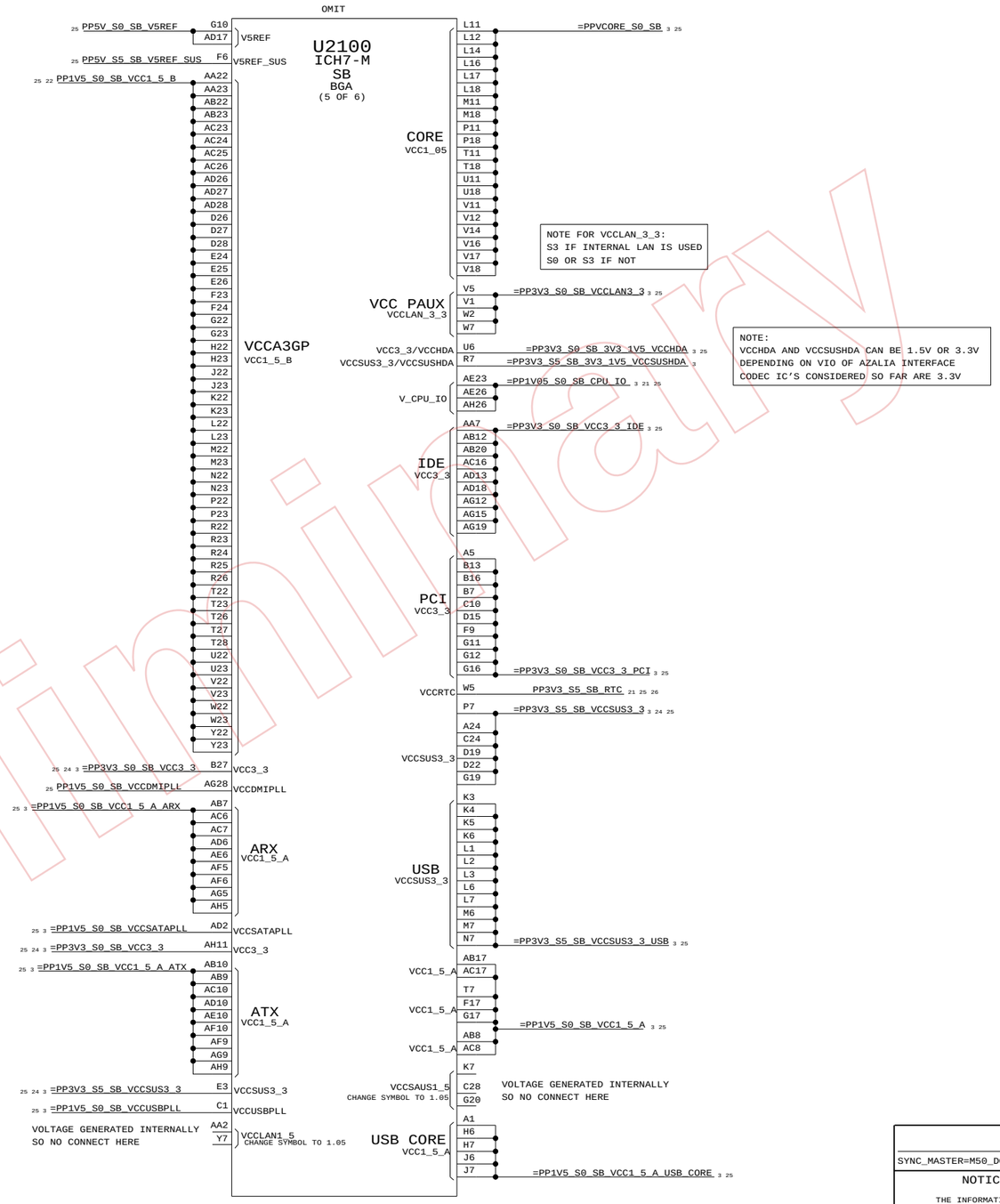
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 23 OF 97	





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SB: 4 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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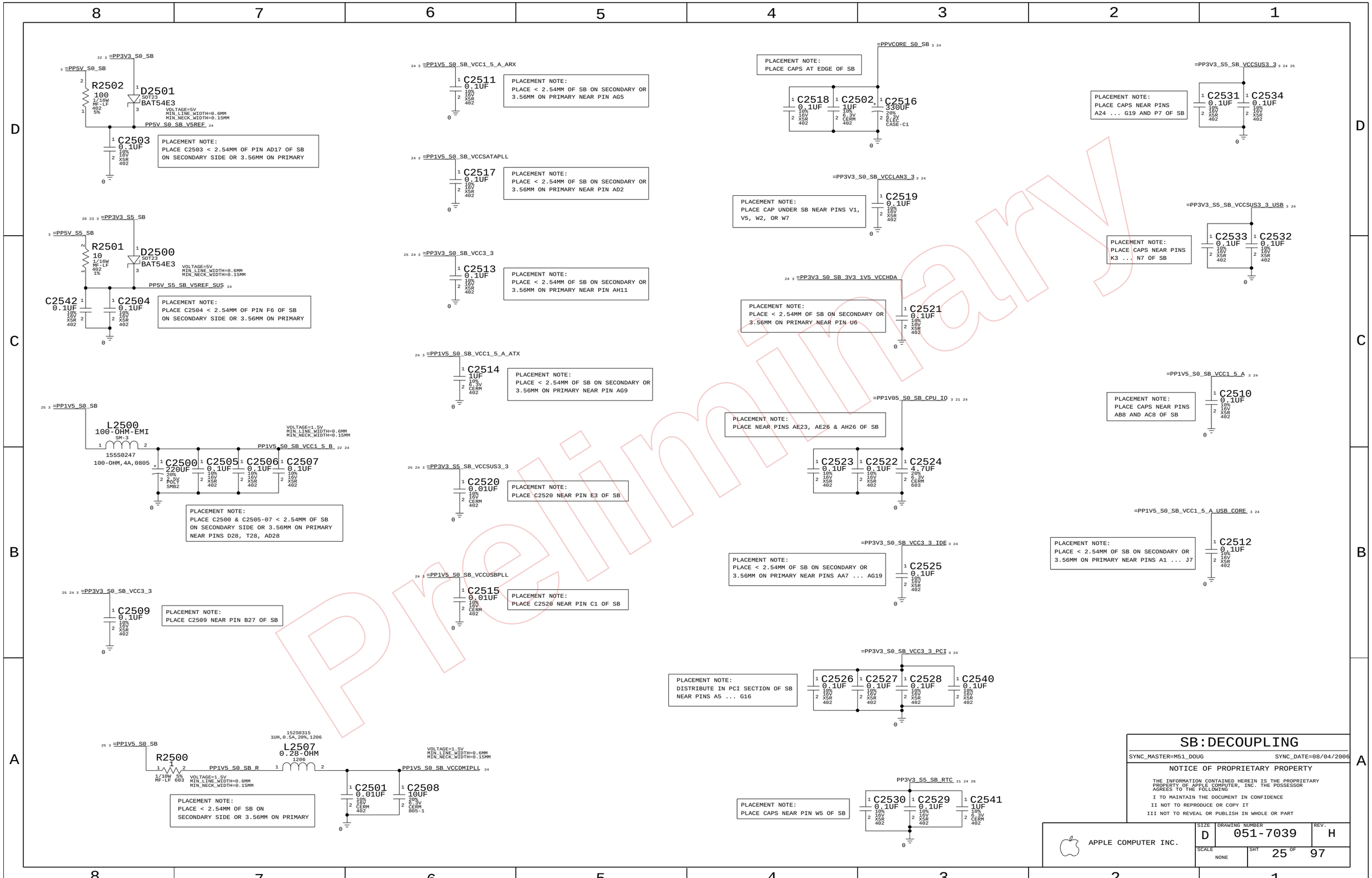
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 24 OF 97	


=PP3V3_S0_SB
=PP5V_S0_SB
R2502
100
1/16W
MF-LF
402
5%
D2501
SOT23
BAT54E3
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
PP5V_S0_SB_V5REF
C2503
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
=PP3V3_S5_SB
=PP5V_S5_SB
R2501
10
1/16W
MF-LF
402
1%
D2500
SOT23
BAT54E3
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
PP5V_S5_SB_V5REF_SUS
C2542
0.1UF
10%
16V
X5R
402
C2504
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
=PP1V5_S0_SB
L2500
100-OHM-EMI
SM-3
155S0247
100-OHM,4A,0805
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
PP1V5_S0_SB_VCC1_5_B
C2500
220UF
20%
2.5V
POLY
SMB2
C2505
0.1UF
10%
16V
X5R
402
C2506
0.1UF
10%
16V
X5R
402
C2507
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
=PP3V3_S0_SB_VCC3_3
C2509
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
=PP1V5_S0_SB
R2500
1/10W 5%
MF-LF 603
PP1V5_S0_SB_R
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
15250315
1UH,0.5A,20%,1206
L2507
0.28-OHM
1206
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
PP1V5_S0_SB_VCCDMIPLL
C2501
0.01UF
10%
16V
CERM
402
C2508
10UF
20%
6.3V
CERM
805-1
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
=PP1V5_S0_SB_VCC1_5_A_ARX
C2511
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
=PP1V5_S0_SB_VCCSATAPLL
C2517
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
=PP3V3_S0_SB_VCC3_3
C2513
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
=PP1V5_S0_SB_VCC1_5_A_ATX
C2514
1UF
10%
6.3V
CERM
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
=PP3V3_S5_SB_VCCSUS3_3
C2520
0.01UF
10%
16V
CERM
402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
=PP1V5_S0_SB_VCCUSBPLL
C2515
0.01UF
10%
16V
CERM
402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
=PPVCORE_S0_SB
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
C2518
0.1UF
10%
16V
X5R
402
C2502
1UF
10%
6.3V
CERM
402
C2516
330UF
20%
2.5V
ELEC
CASE-C1
=PP3V3_S0_SB_VCCLAN3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V1,
V5, W2, OR W7
C2519
0.1UF
10%
16V
X5R
402
=PP3V3_S0_SB_3V3_1V5_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
C2521
0.1UF
10%
16V
X5R
402
=PP1V05_S0_SB_CPU_IO
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523
0.1UF
10%
16V
X5R
402
C2522
0.1UF
10%
16V
X5R
402
C2524
4.7UF
20%
6.3V
CERM
603
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7 ... AG19
C2525
0.1UF
10%
16V
X5R
402
=PP3V3_S0_SB_VCC3_3_PCI
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526
0.1UF
10%
16V
X5R
402
C2527
0.1UF
10%
16V
X5R
402
C2528
0.1UF
10%
16V
X5R
402
C2540
0.1UF
10%
16V
X5R
402
PP3V3_S5_SB_RTC
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530
0.1UF
10%
16V
X5R
402
C2529
0.1UF
10%
16V
X5R
402
C2541
1UF
10%
6.3V
CERM
402
=PP3V3_S5_SB_VCCSUS3_3
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531
0.1UF
10%
16V
X5R
402
C2534
0.1UF
10%
16V
X5R
402
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533
0.1UF
10%
16V
X5R
402
C2532
0.1UF
10%
16V
X5R
402
=PP1V5_S0_SB_VCC1_5_A
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510
0.1UF
10%
16V
X5R
402
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... J7
C2512
0.1UF
10%
16V
X5R
402
Preliminary
SB:DECOUPLING
SYNC_MASTER=M51_DOUG
SYNC_DATE=08/04/2006
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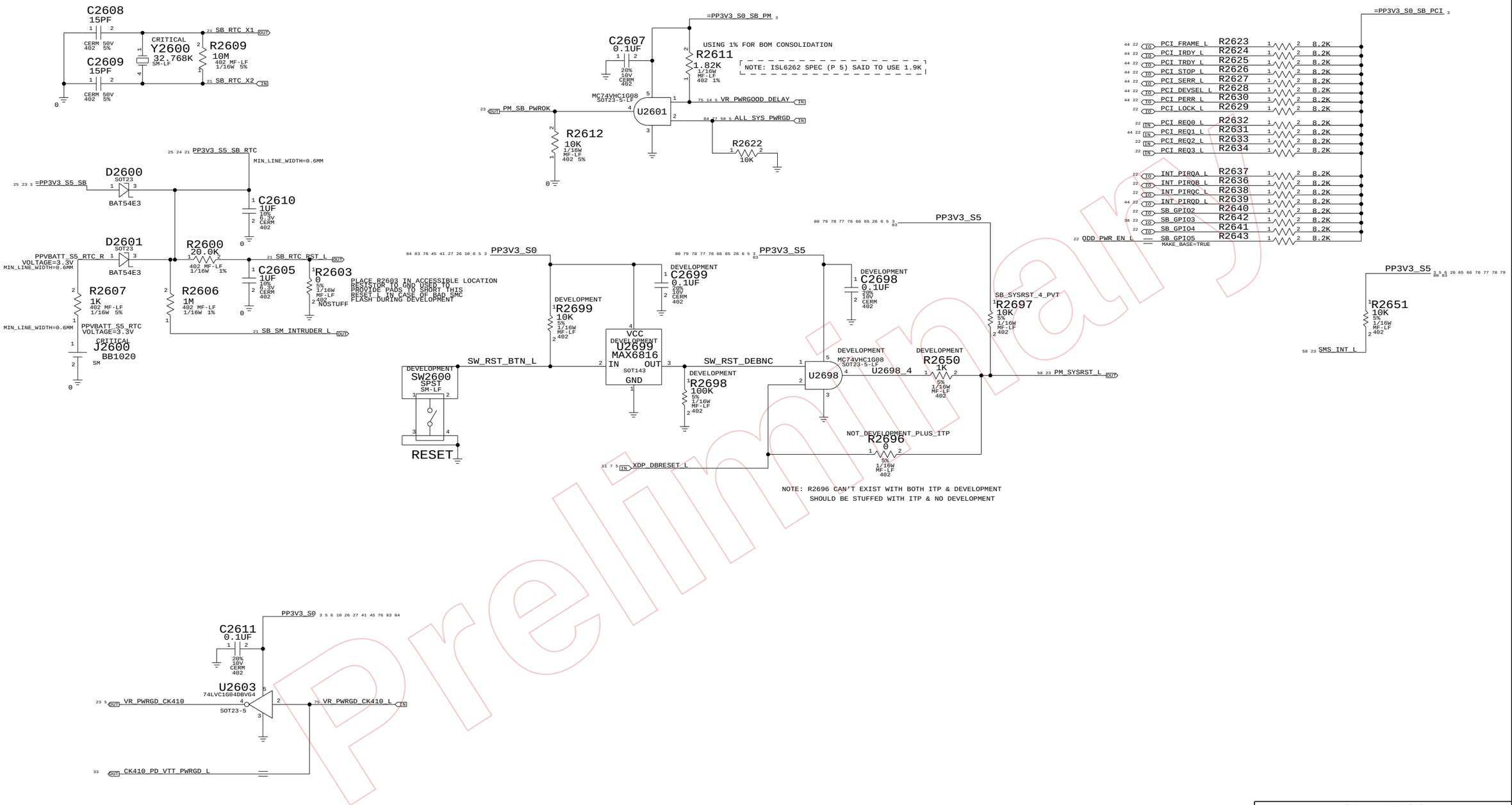
SIZE D
DRAWING NUMBER 051-7039
REV. H
SCALE NONE
SHT 25 OF 97



Preliminary

SB: MISC

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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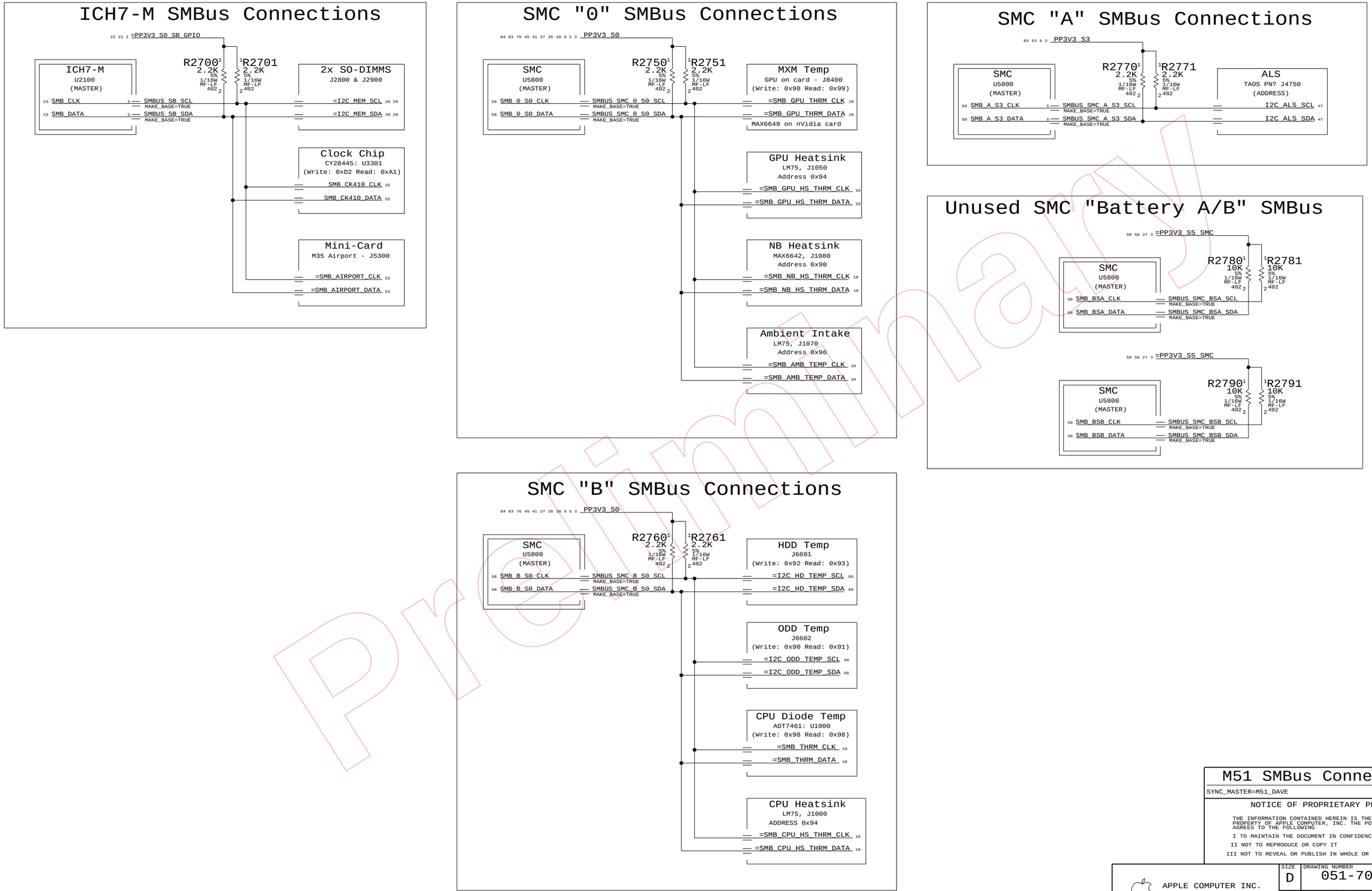
SCALE NONE	SHT 26 OF 97	



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M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 27 OF 97	

Page Notes

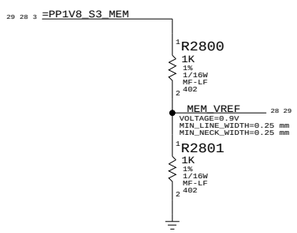
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

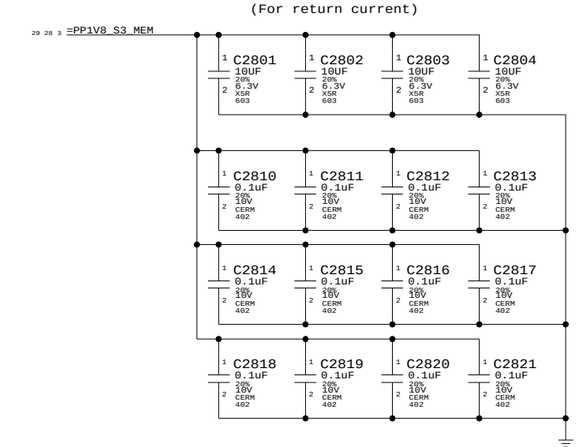
DDR2 VRef

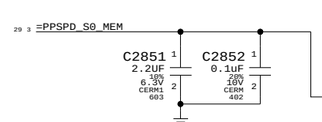
One 0.1uF per connector



DDR2 Bypass Caps

(For return current)





DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 28 OF 97	

Preliminary

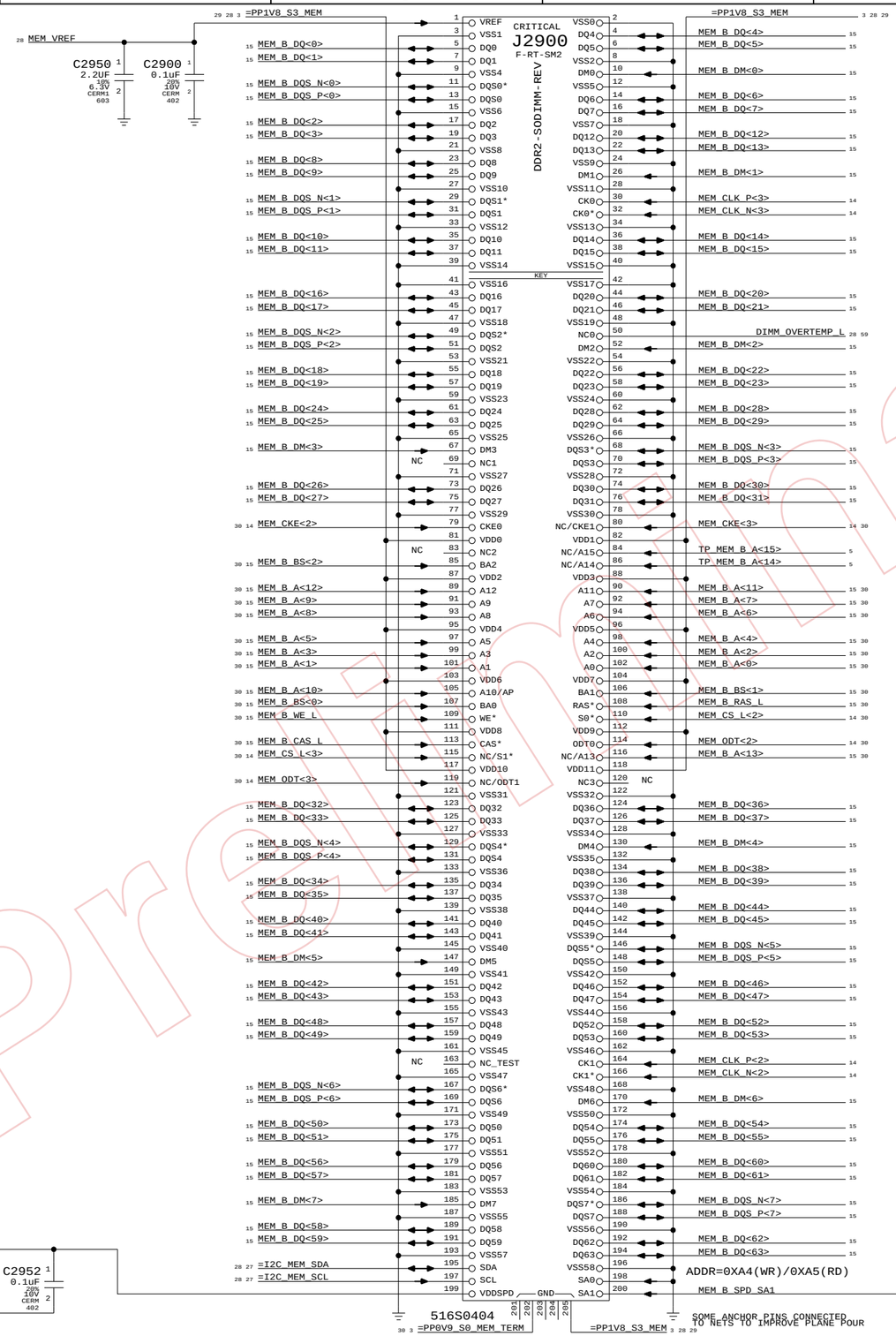
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

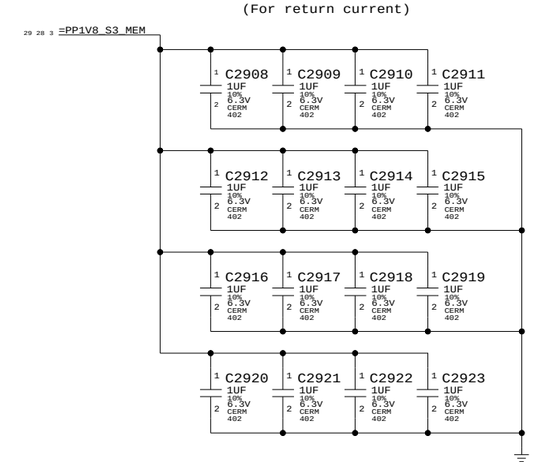
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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SIZE	DRAWING NUMBER	REV.
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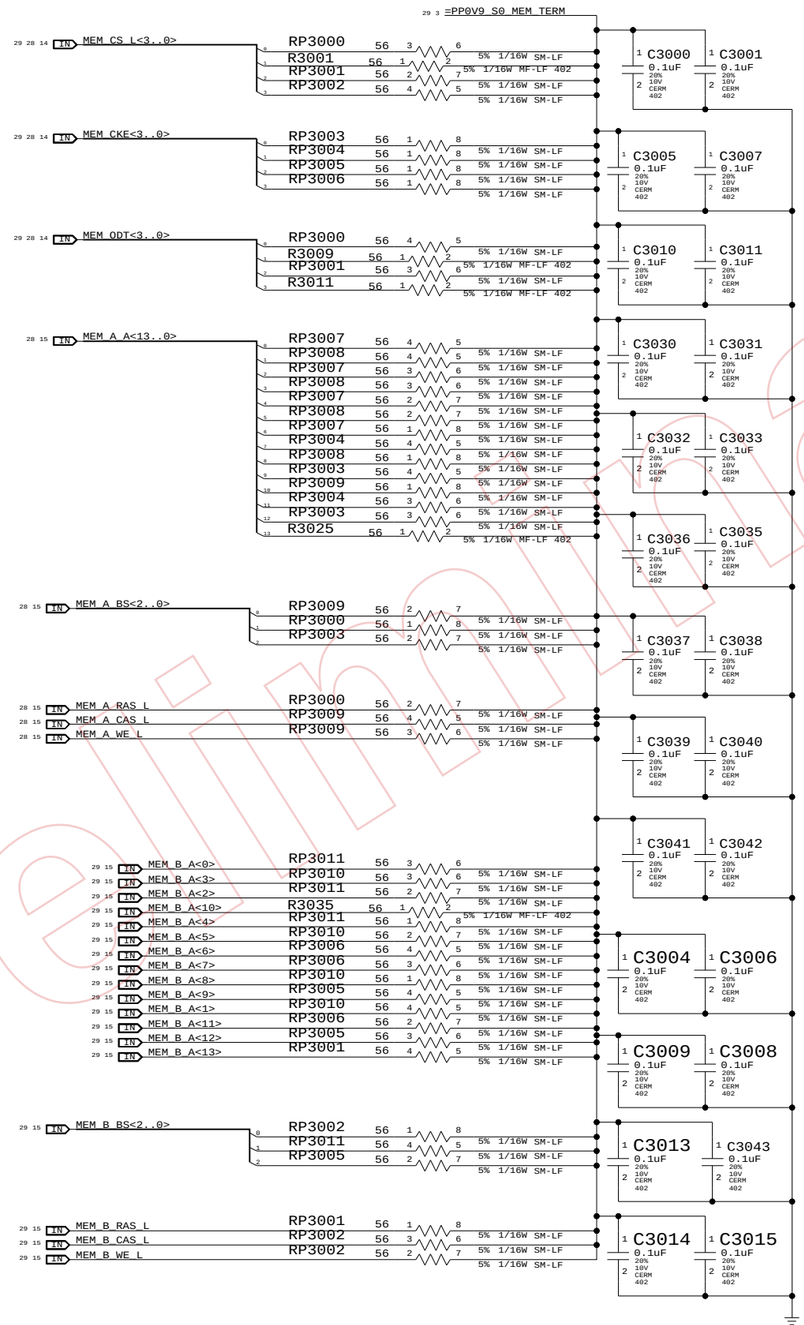
Preliminary

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Preliminary

Memory Active Termination

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 30 OF 97	

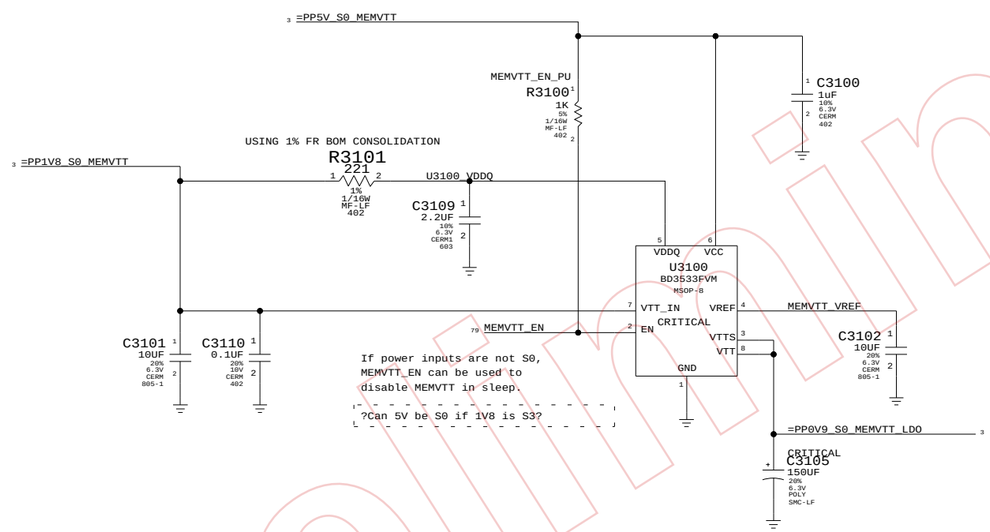
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Preliminary

Memory Vtt Supply

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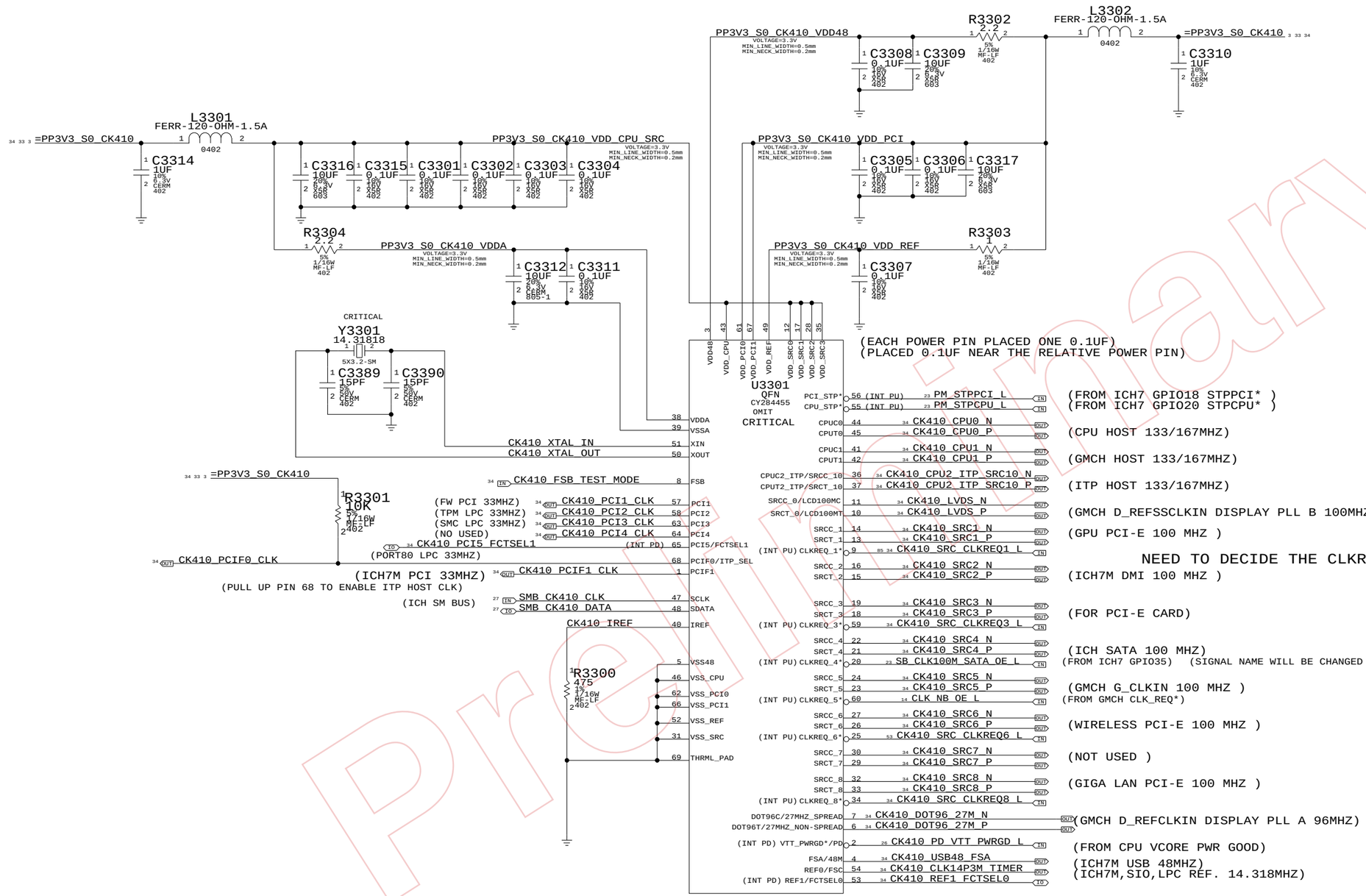

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

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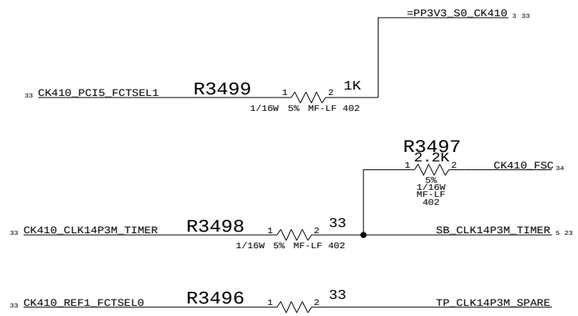
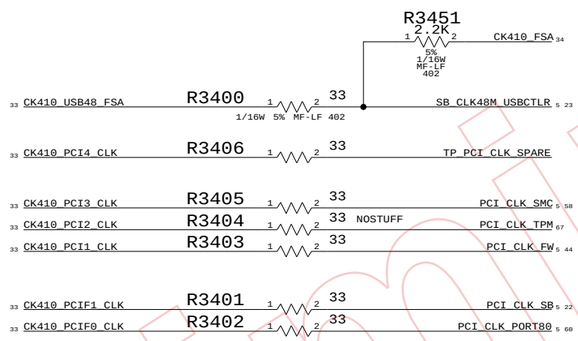
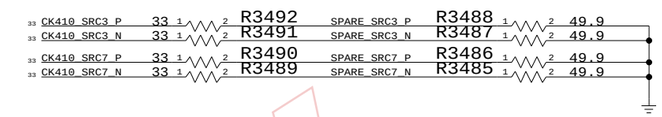
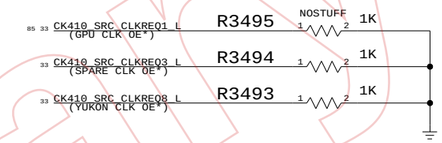






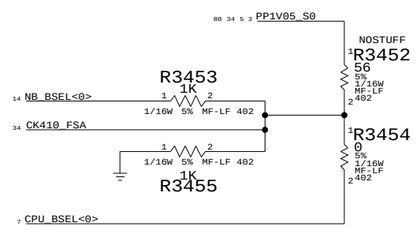
NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

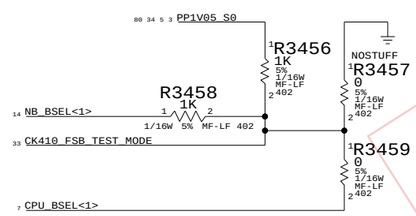


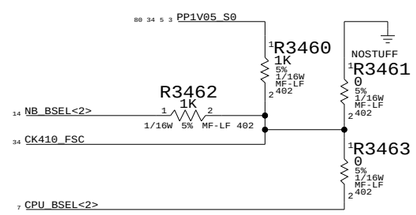
NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

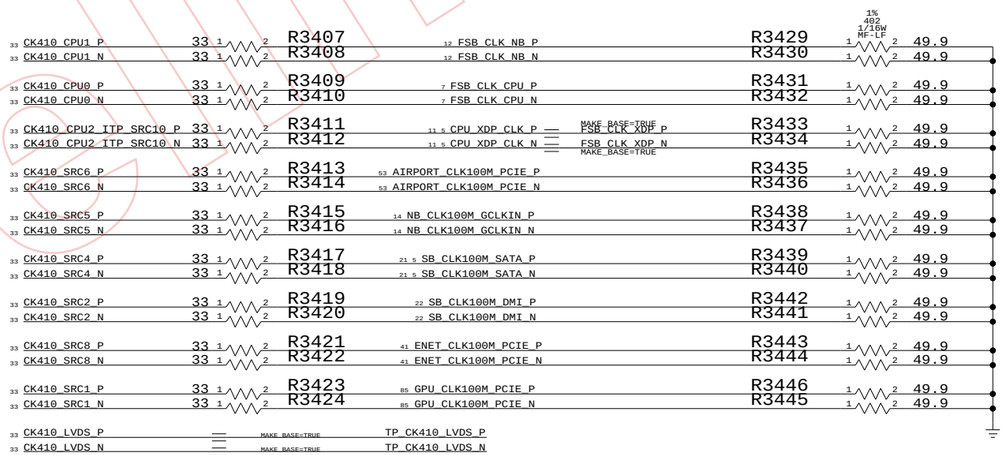
FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

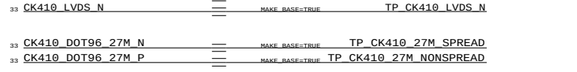








TPM CLOCK IS TURNED OFF IN SW AND RESISTOR NOSTUFF



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CLOCKS: TERMINATIONS

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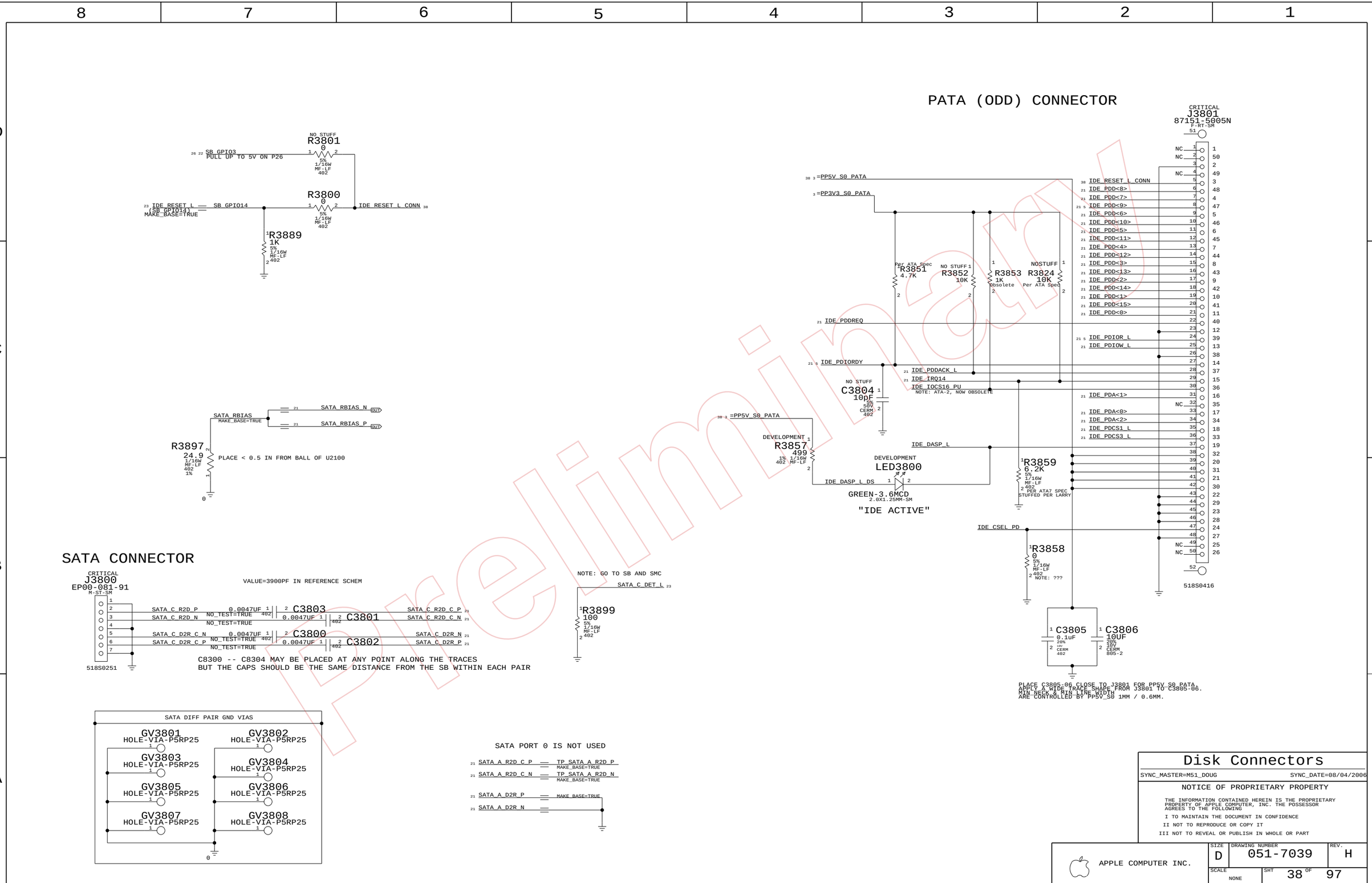
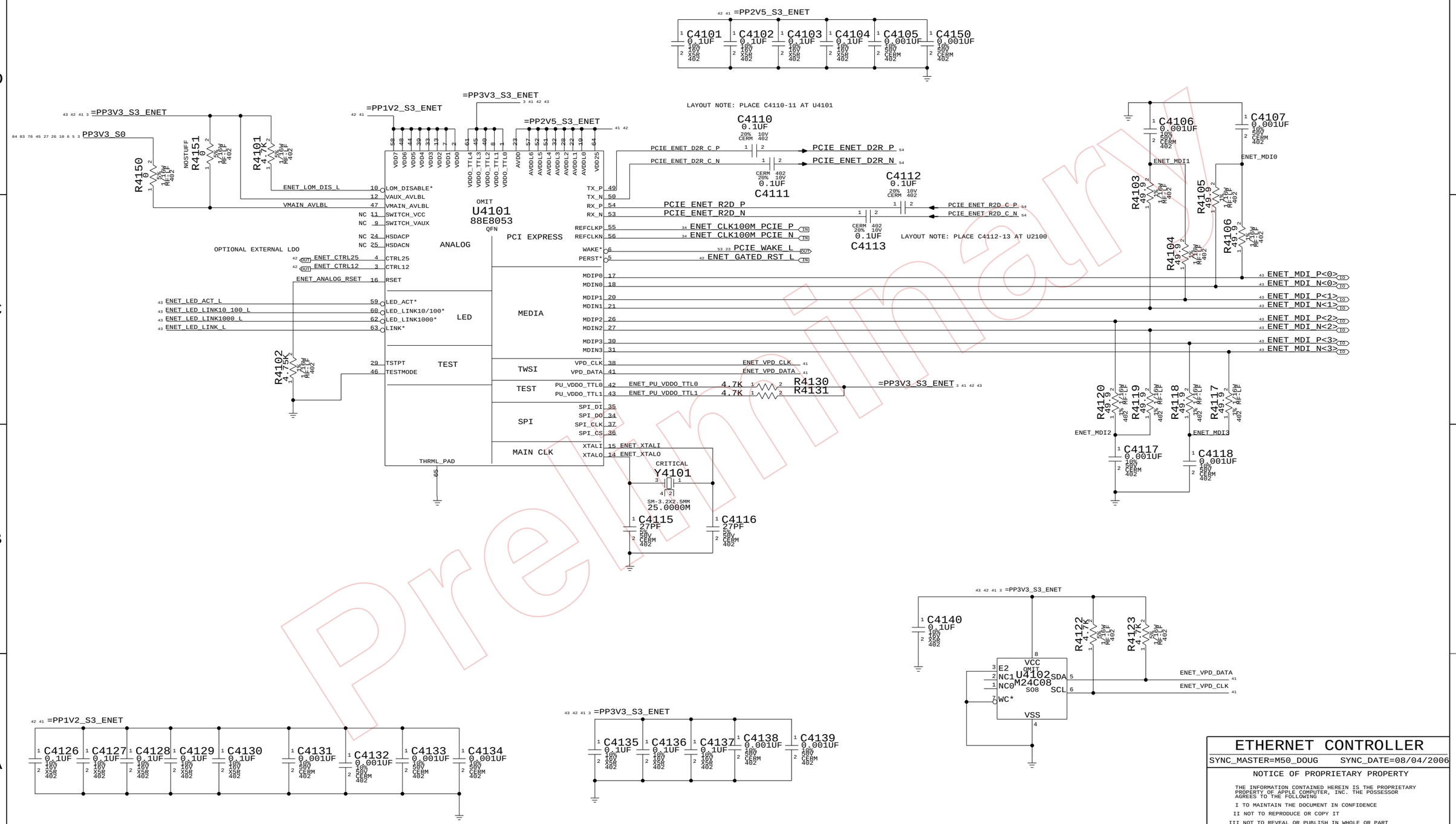
SCALE NONE	SHT 34 OF 97	



Preliminary



ETHERNET CONTROLLER

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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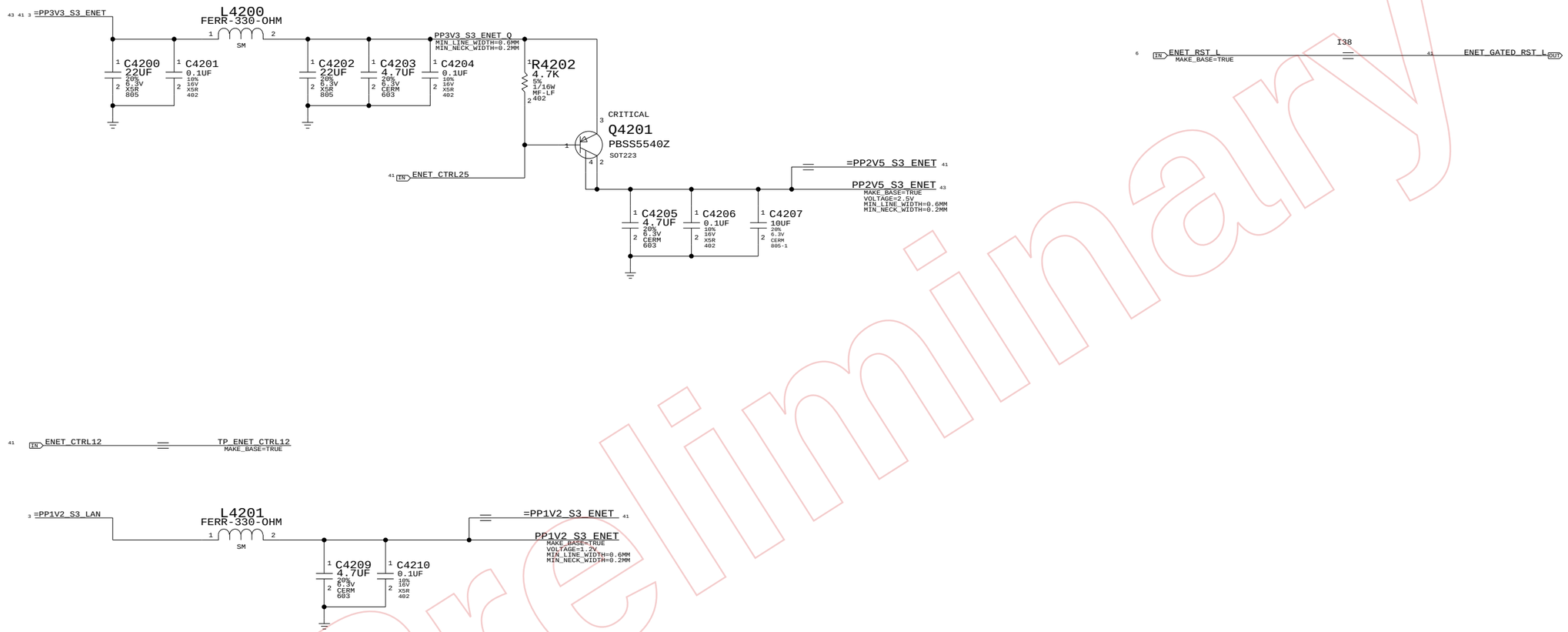

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ETHERNET MISC

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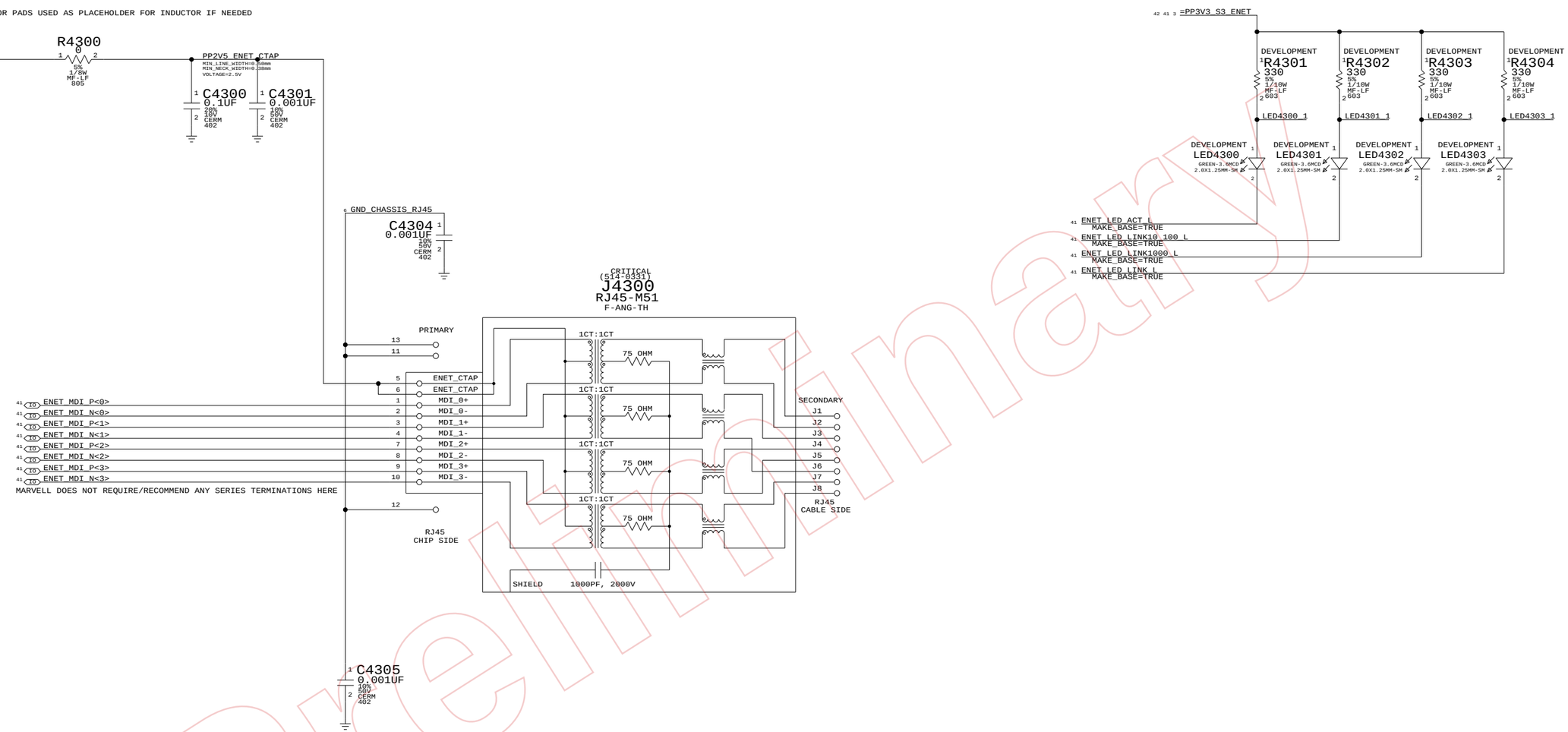

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ETHERNET CONNECTOR

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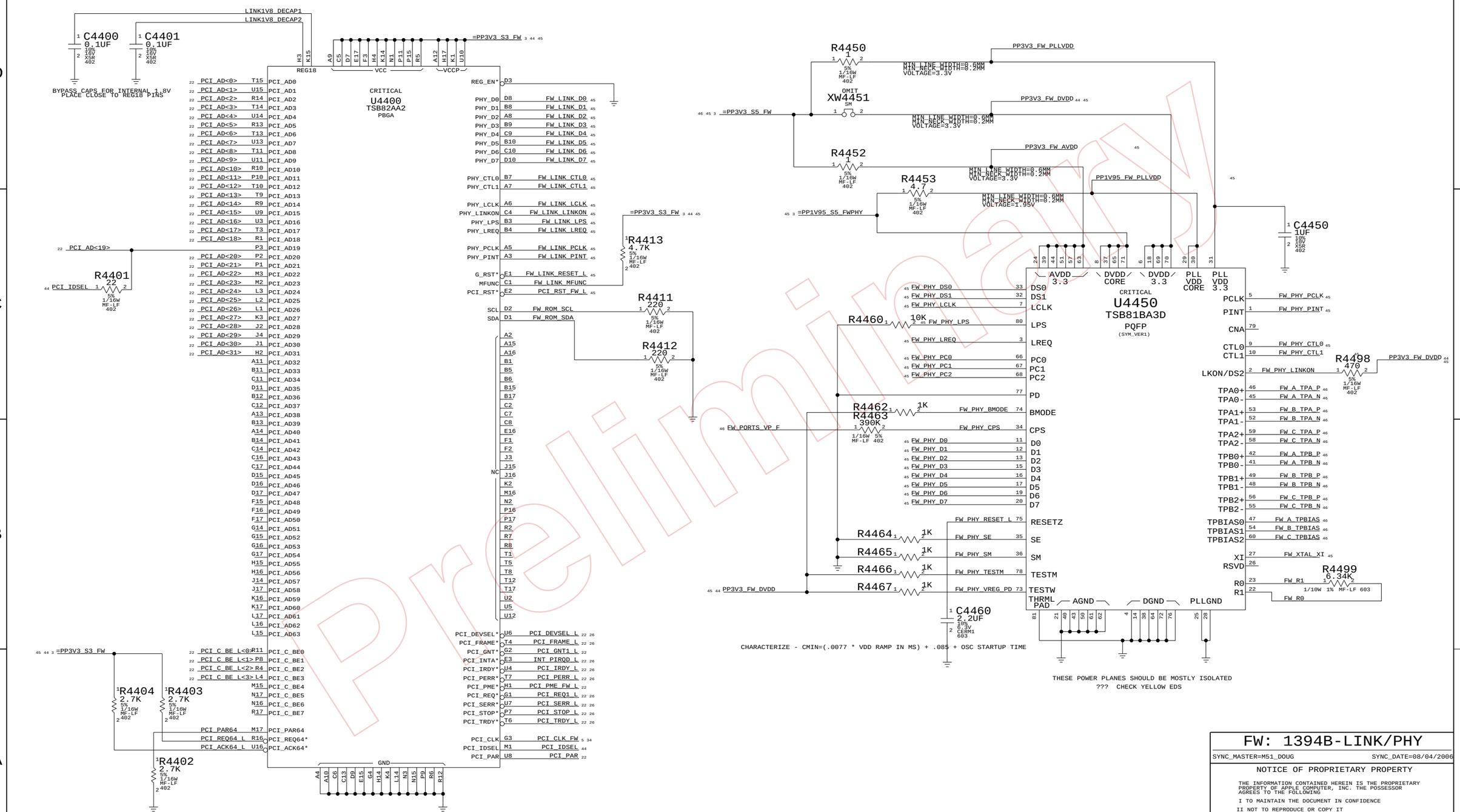
SCALE NONE	SHT 43 OF 97	



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FW: 1394B-LINK/PHY

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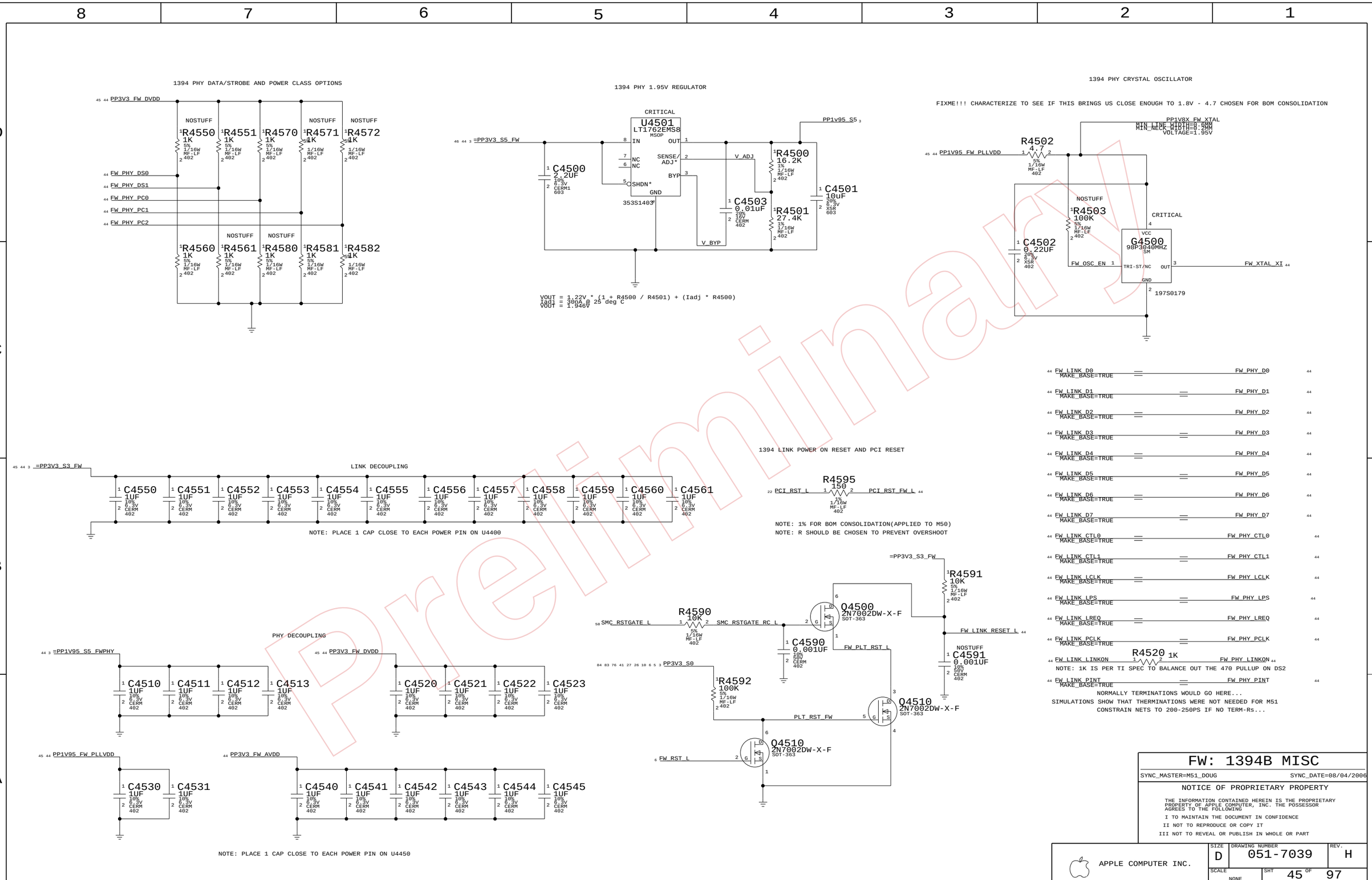
1394 PHY DATA/STROBE AND POWER CLASS OPTIONS
PP3V3_FW_DVDD
NOSTUFF
R4550 1K
R4551 1K
R4570 1K
R4571 1K
R4572 1K
FW_PHY_DS0
FW_PHY_DS1
FW_PHY_PC0
FW_PHY_PC1
FW_PHY_PC2
R4560 1K
R4561 1K
R4580 1K
R4581 1K
R4582 1K
1394 PHY 1.95V REGULATOR
CRITICAL
U4501
LT1762EMS8
MSOP
=PP3V3_S5_FW
PP1v95_S5
IN
OUT
NC
SENSE/ADJ*
V_ADJ
SHDN*
BYP
GND
353S1403
C4500 2.2UF
R4500 16.2K
R4501 27.4K
C4503 0.01UF
C4501 10uF
V_BYP
VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V
1394 PHY CRYSTAL OSCILLATOR
FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION
PP1V8X_FW_XTAL
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.95V
R4502 4.7
PP1V95_FW_PLLVDD
R4503 100K
C4502 0.22UF
CRITICAL
G4500
98P3040MHZ
VCC
TRI-ST/NC
OUT
GND
FW_OSC_EN
FW_XTAL_XI
197S0179
FW_LINK_D0
FW_LINK_D1
FW_LINK_D2
FW_LINK_D3
FW_LINK_D4
FW_LINK_D5
FW_LINK_D6
FW_LINK_D7
FW_LINK_CTL0
FW_LINK_CTL1
FW_LINK_LCLK
FW_LINK_LPS
FW_LINK_LREQ
FW_LINK_PCLK
FW_LINK_LINKON
FW_LINK_PINT
MAKE_BASE=TRUE
FW_PHY_D0
FW_PHY_D1
FW_PHY_D2
FW_PHY_D3
FW_PHY_D4
FW_PHY_D5
FW_PHY_D6
FW_PHY_D7
FW_PHY_CTL0
FW_PHY_CTL1
FW_PHY_LCLK
FW_PHY_LPS
FW_PHY_LREQ
FW_PHY_PCLK
FW_PHY_LINKON
FW_PHY_PINT
R4520 1K
NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2
NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...
LINK DECOUPLING
=PP3V3_S3_FW
C4550 1UF
C4551 1UF
C4552 1UF
C4553 1UF
C4554 1UF
C4555 1UF
C4556 1UF
C4557 1UF
C4558 1UF
C4559 1UF
C4560 1UF
C4561 1UF
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400
1394 LINK POWER ON RESET AND PCI RESET
R4595 150
PCI_RST_L
PCI_RST_FW_L
NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT
=PP3V3_S3_FW
R4591 10K
Q4500 2N7002DW-X-F
SOT-363
R4590 10K
SMC_RSTGATE_L
SMC_RSTGATE_RC_L
C4590 0.001UF
FW_LINK_RESET_L
NOSTUFF
C4591 0.001UF
FW_PLT_RST_L
PP3V3_S0
R4592 100K
Q4510 2N7002DW-X-F
PLT_RST_FW
FW_RST_L
PHY DECOUPLING
=PP1V95_S5_FWPHY
PP3V3_FW_DVDD
C4510 1UF
C4511 1UF
C4512 1UF
C4513 1UF
C4520 1UF
C4521 1UF
C4522 1UF
C4523 1UF
PP1V95_FW_PLLVDD
PP3V3_FW_AVDD
C4530 1UF
C4531 1UF
C4540 1UF
C4541 1UF
C4542 1UF
C4543 1UF
C4544 1UF
C4545 1UF
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450
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FW: 1394B MISC
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SYNC_DATE=08/04/2006
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DRAWING NUMBER 051-7039
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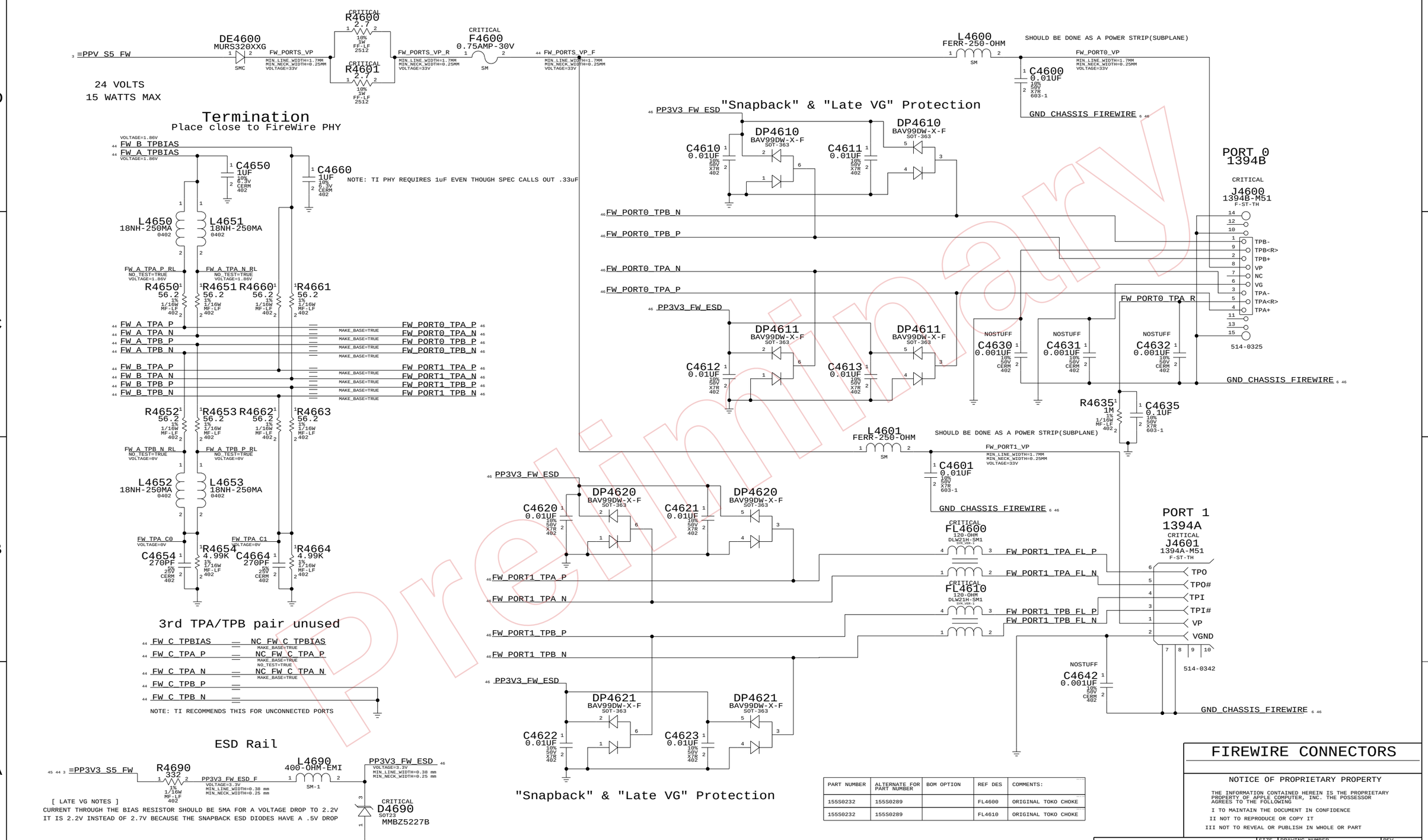
SCALE NONE
SHT 45 OF 97



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

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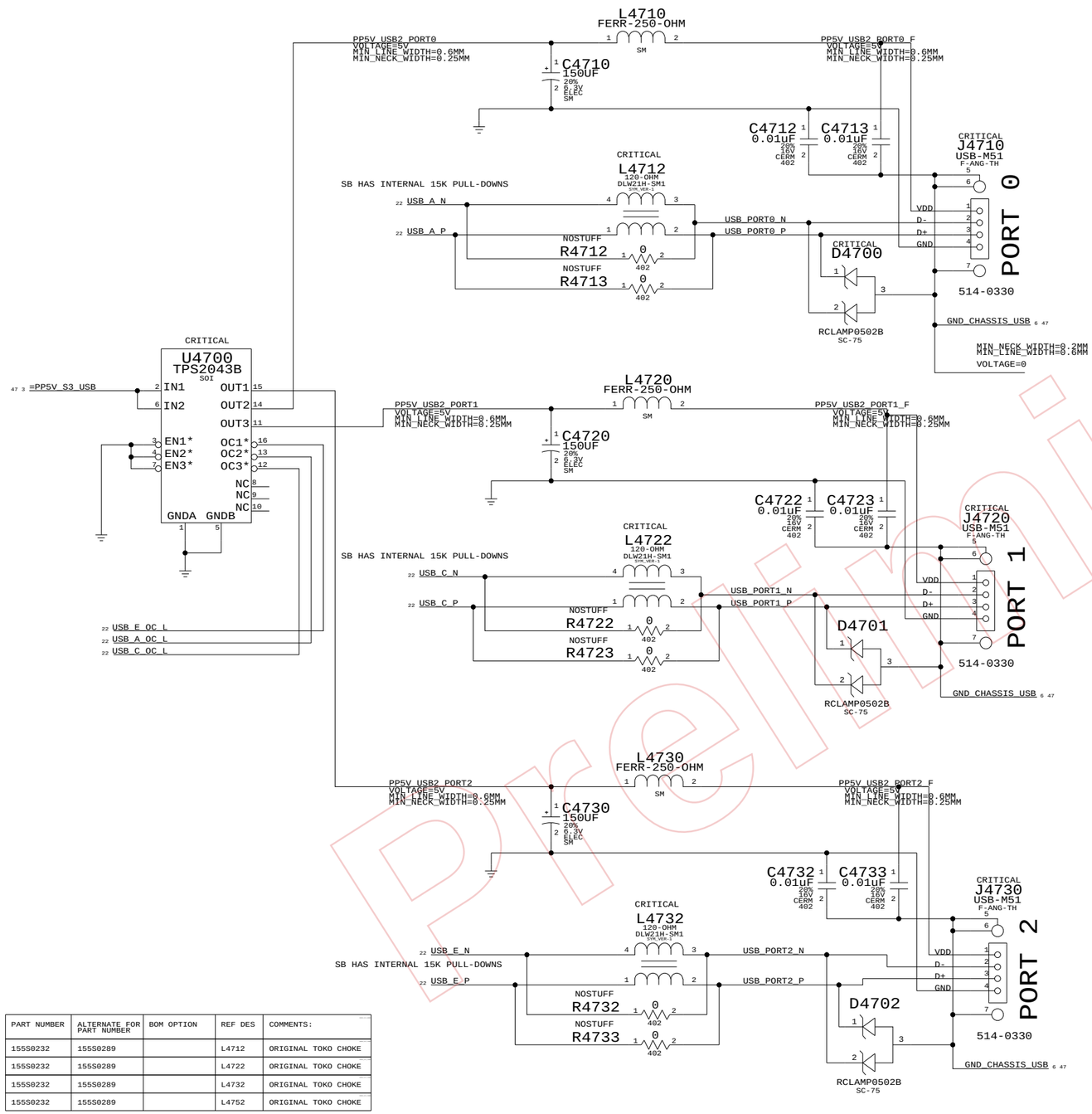
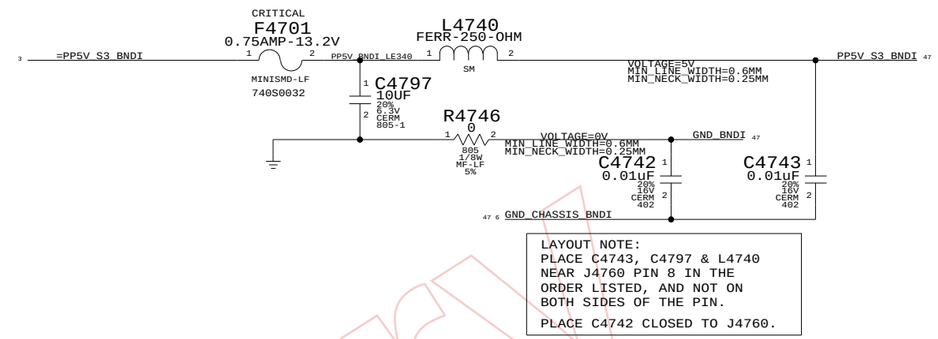
External USB Ports



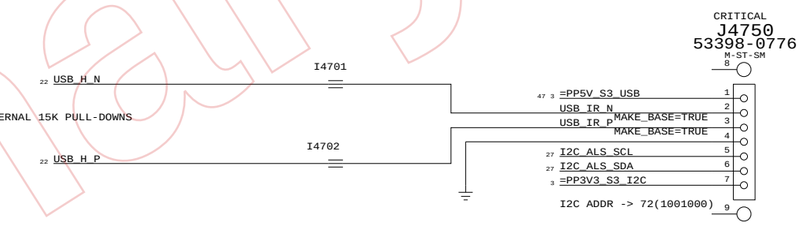
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



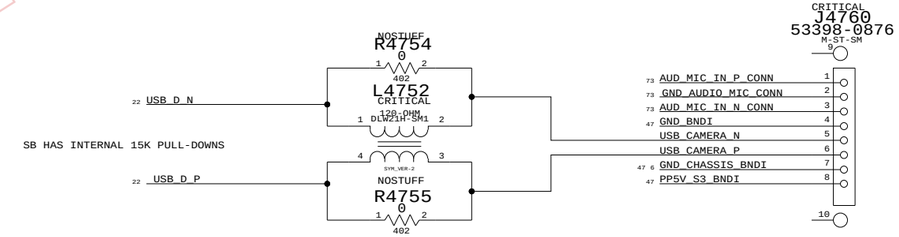
LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR J4760 PIN 8 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO J4760.

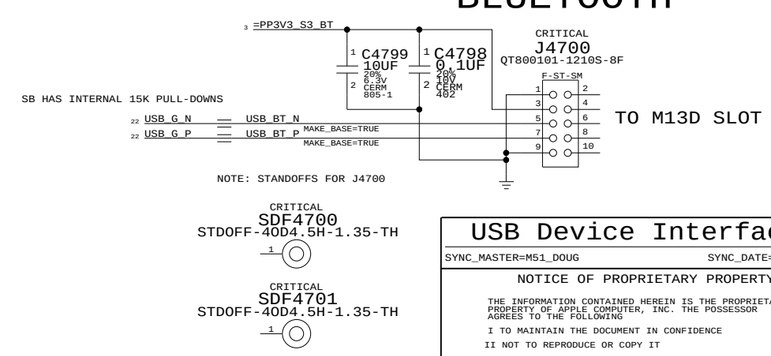
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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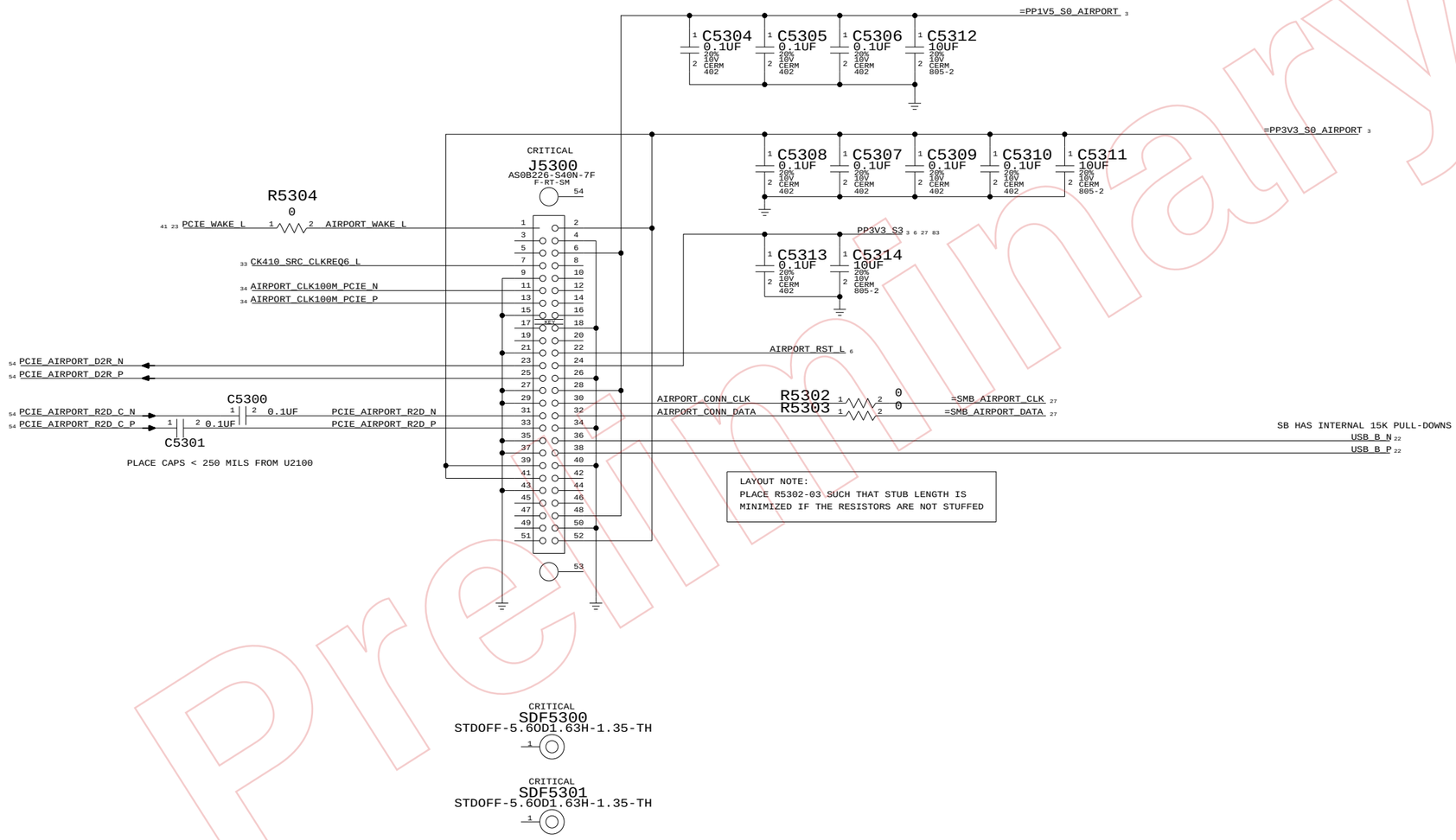

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AIRPORT CONN

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SCALE NONE	SHT 53 OF 97	

PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

Preliminary

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=08/04/2006

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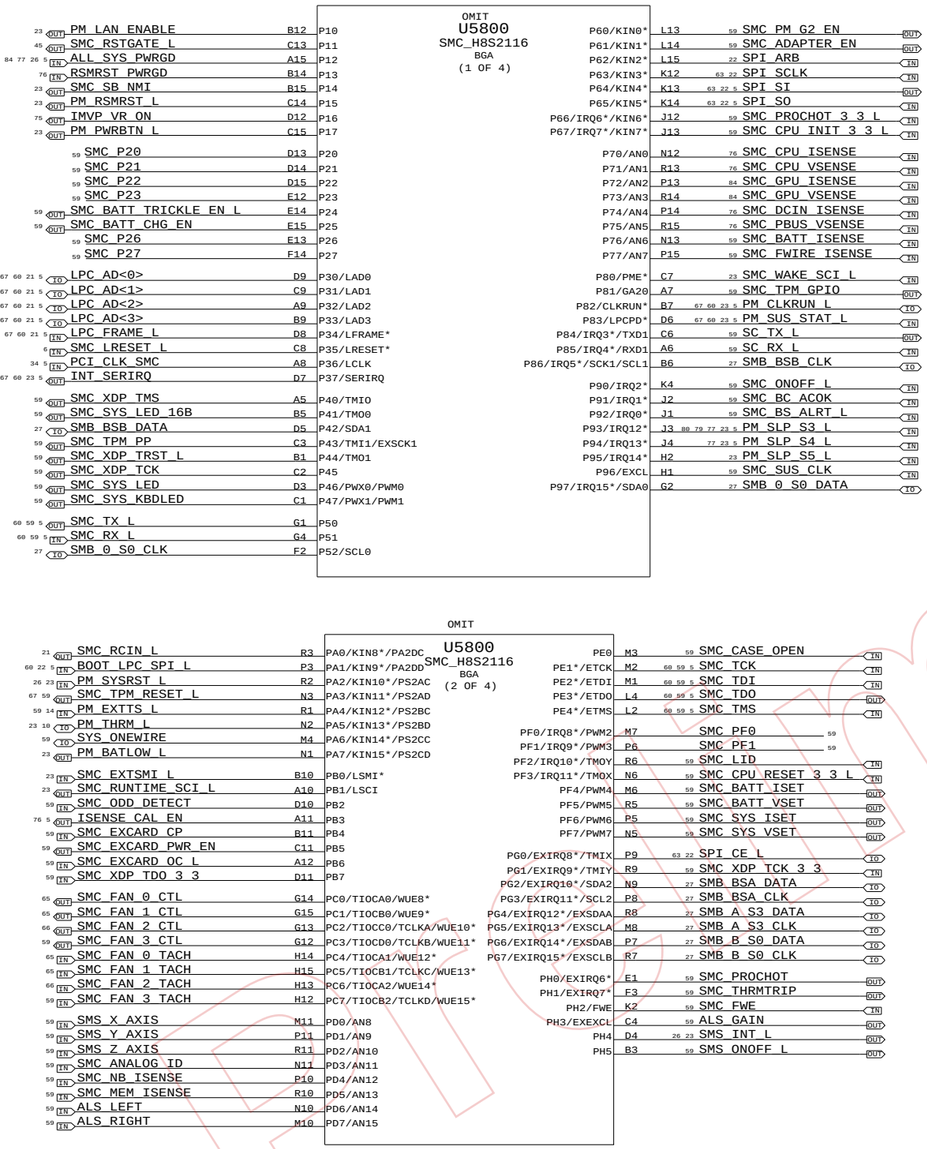
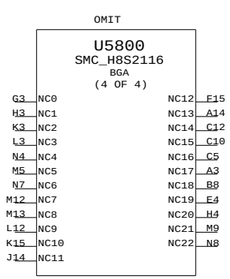
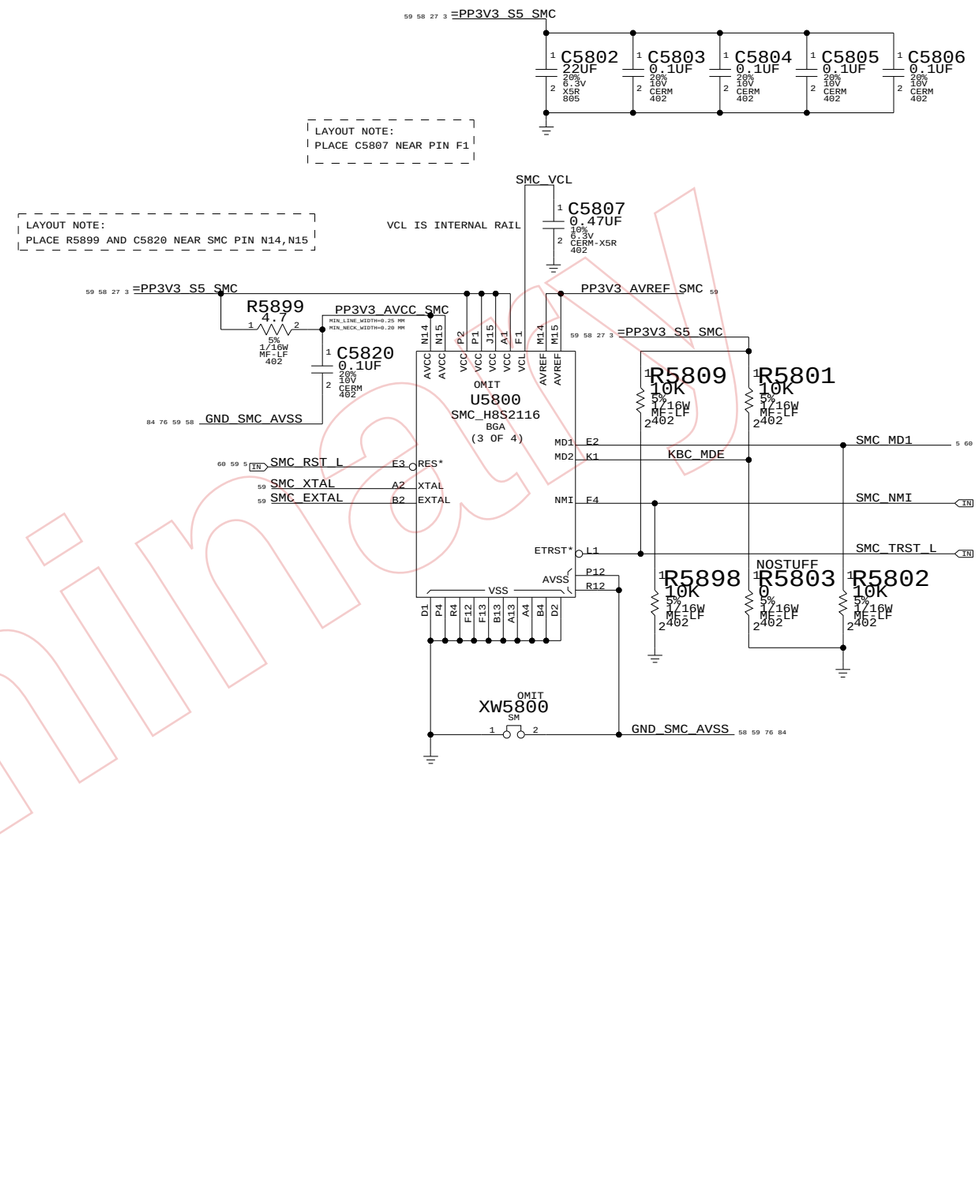
UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.







SMC

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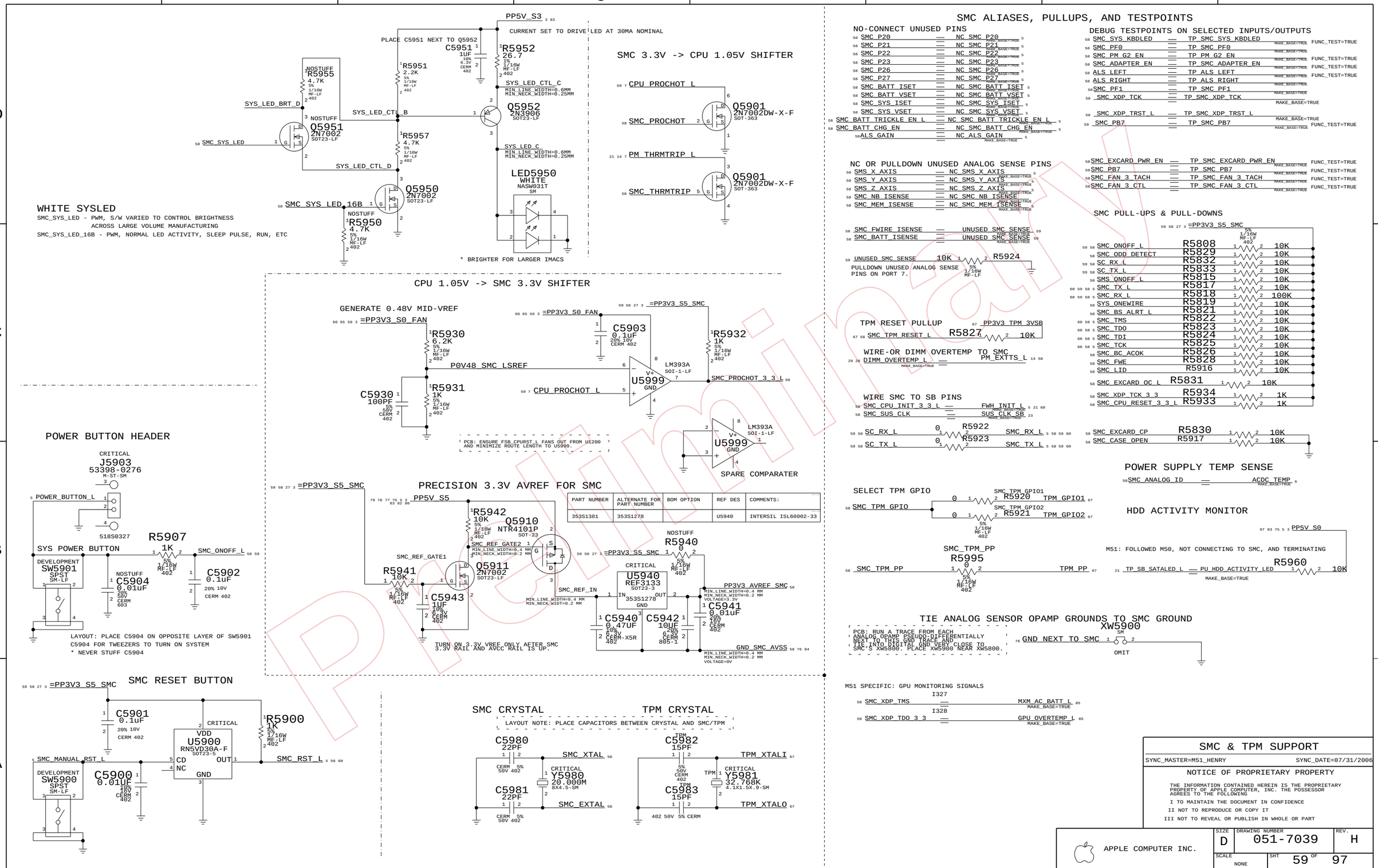
Preliminary


WHITE SYSLED
SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS ACROSS LARGE VOLUME MANUFACTURING
SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC
PP5V_S3
CURRENT SET TO DRIVE LED AT 30MA NOMINAL
PLACE C5951 NEXT TO Q5952
C5951 1UF
R5952 26.7
R5955 4.7K
R5951 2.2K
R5957 4.7K
Q5951 2N7002
Q5952 2N3906
Q5950 2N7002
R5950 4.7K
LED5950 WHITE NASW031T
* BRIGHTER FOR LARGER IMACS
SMC 3.3V -> CPU 1.05V SHIFTER
Q5901 2N7002DW-X-F
CPU 1.05V -> SMC 3.3V SHIFTER
GENERATE 0.48V MID-VREF
R5930 6.2K
R5931 1K
C5930 100PF
C5903 0.1UF
R5932 1K
U5999 LM393A
SPARE COMPARATOR
PRECISION 3.3V AVREF FOR SMC
R5942 10K
Q5910 NTR4101P
Q5911 2N7002
R5941 10K
C5943 1UF
R5940 0
U5940 REF3133
C5940 0.47UF
C5942 10UF
C5941 0.01UF
TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.
POWER BUTTON HEADER
J5903 53398-0276
SYS POWER BUTTON
SW5901
R5907 1K
C5904 0.01UF
C5902 0.1UF
LAYOUT: PLACE C5904 ON OPPOSITE LAYER OF SW5901 C5904 FOR TWEEZERS TO TURN ON SYSTEM
* NEVER STUFF C5904
SMC RESET BUTTON
C5901 0.1UF
U5900 RN5VD30A-F
R5900 1K
SW5900
C5900 0.01UF
SMC CRYSTAL
TPM CRYSTAL
LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM
C5980 22PF
C5981 22PF
Y5980 20.000M
C5982 15PF
C5983 15PF
Y5981 32.768K
SMC ALIASES, PULLUPS, AND TESTPOINTS
NO-CONNECT UNUSED PINS
DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
NC OR PULLDOWN UNUSED ANALOG SENSE PINS
PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.
SMC PULL-UPS & PULL-DOWNS
TPM RESET PULLUP
WIRE-OR DIMM OVERTEMP TO SMC
WIRE SMC TO SB PINS
SELECT TPM GPIO
POWER SUPPLY TEMP SENSE
HDD ACTIVITY MONITOR
M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING
TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND
PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.
M51 SPECIFIC: GPU MONITORING SIGNALS
SMC & TPM SUPPORT
SYNC_MASTER=M51_HENRY
SYNC_DATE=07/31/2006
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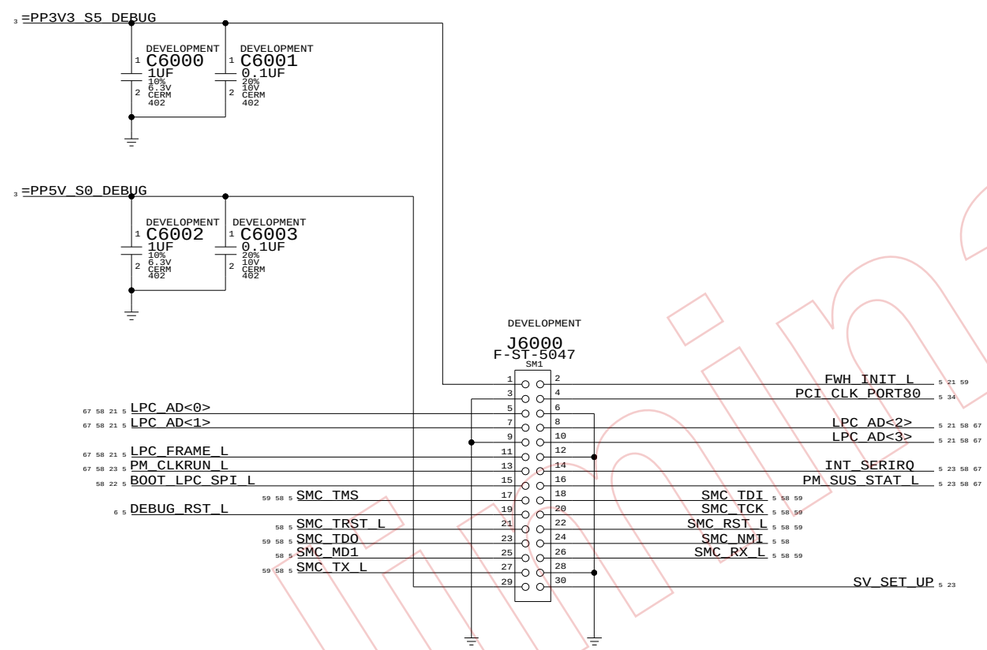
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. H
SCALE NONE
SHT 59 OF 97



Preliminary

LPC+ CONN

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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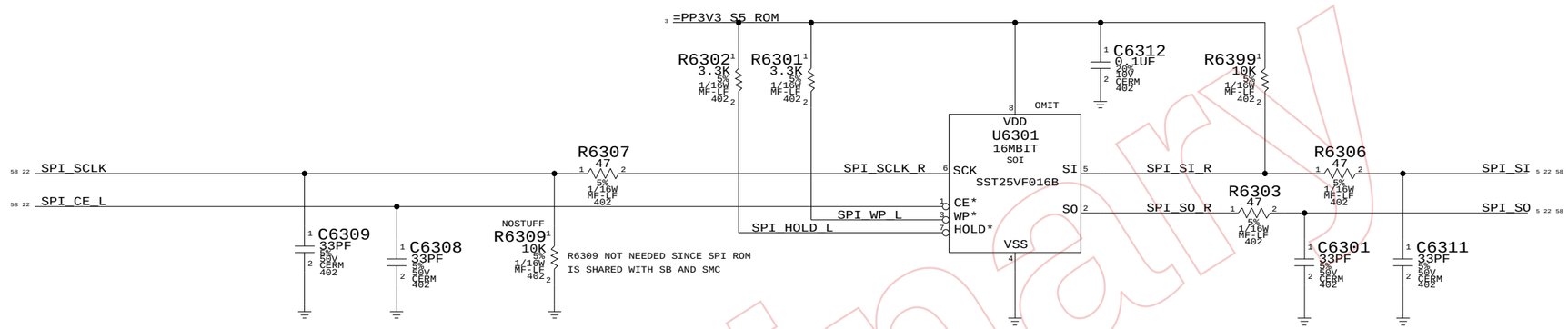
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 60 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

Preliminary

SPI BOOTROM

SYNC_MASTER=M50_DOUG SYNC_DATE=08/04/2006

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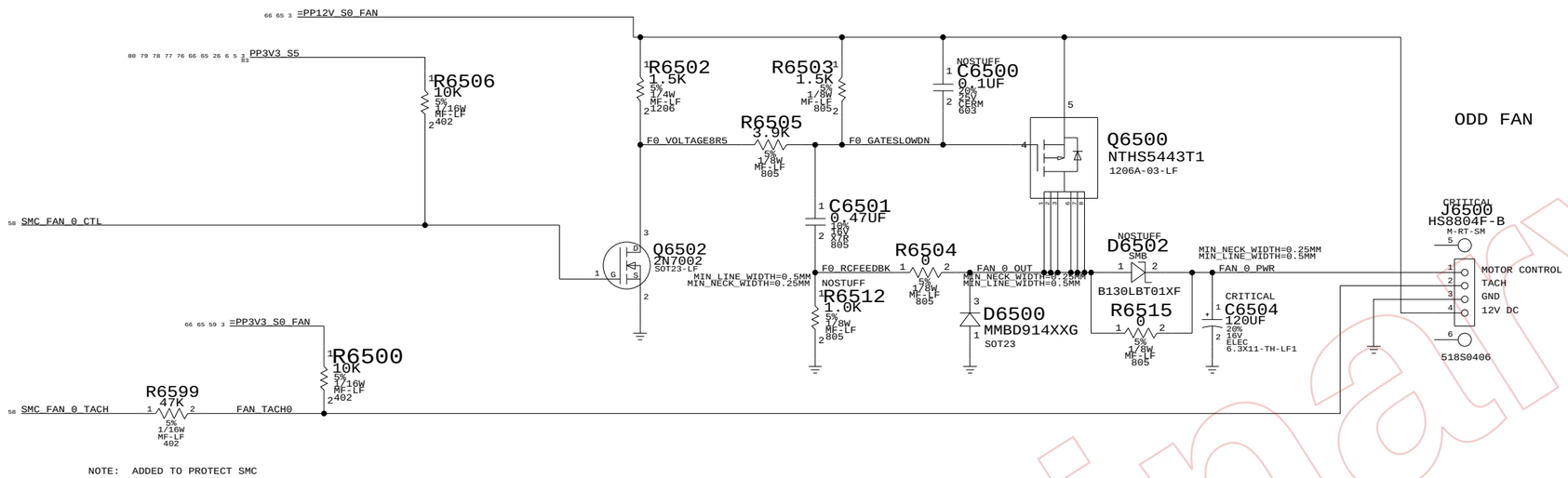
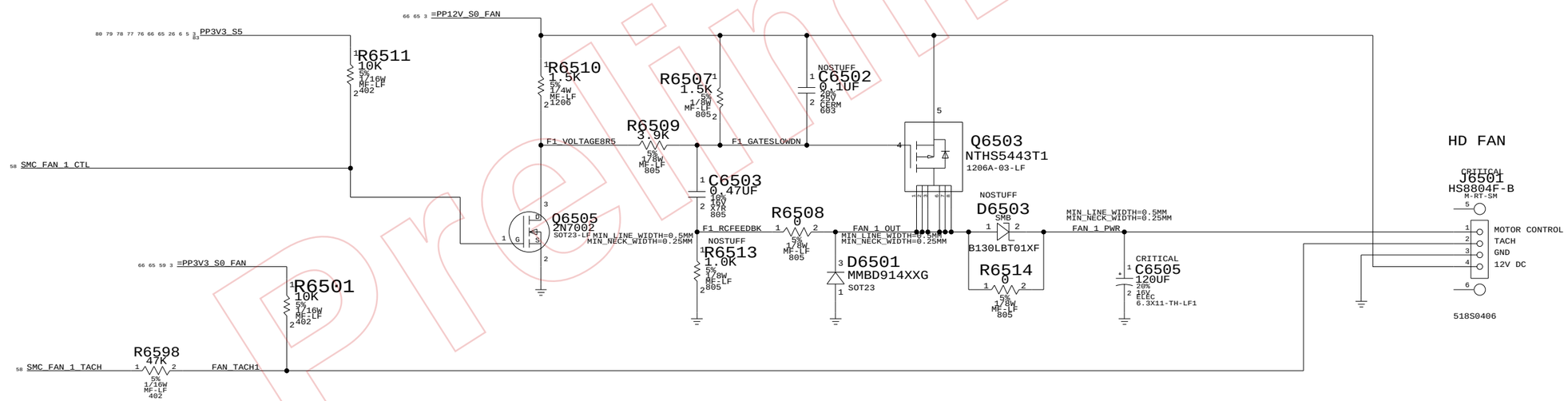
FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



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HD AND OD FAN

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SIZE	DRAWING NUMBER	REV.
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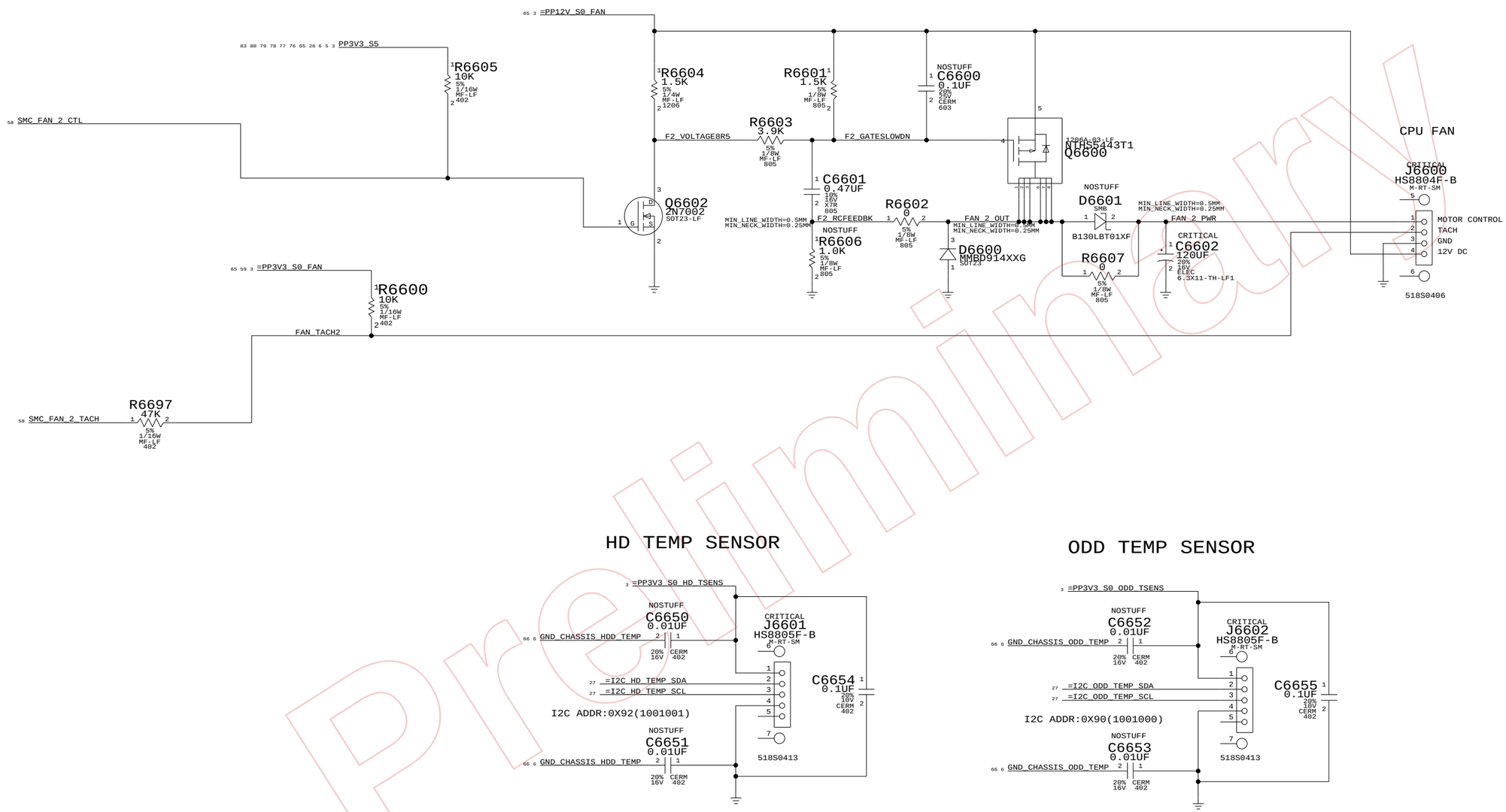
FAN 2



HD TEMP SENSOR

ODD TEMP SENSOR

Preliminary

CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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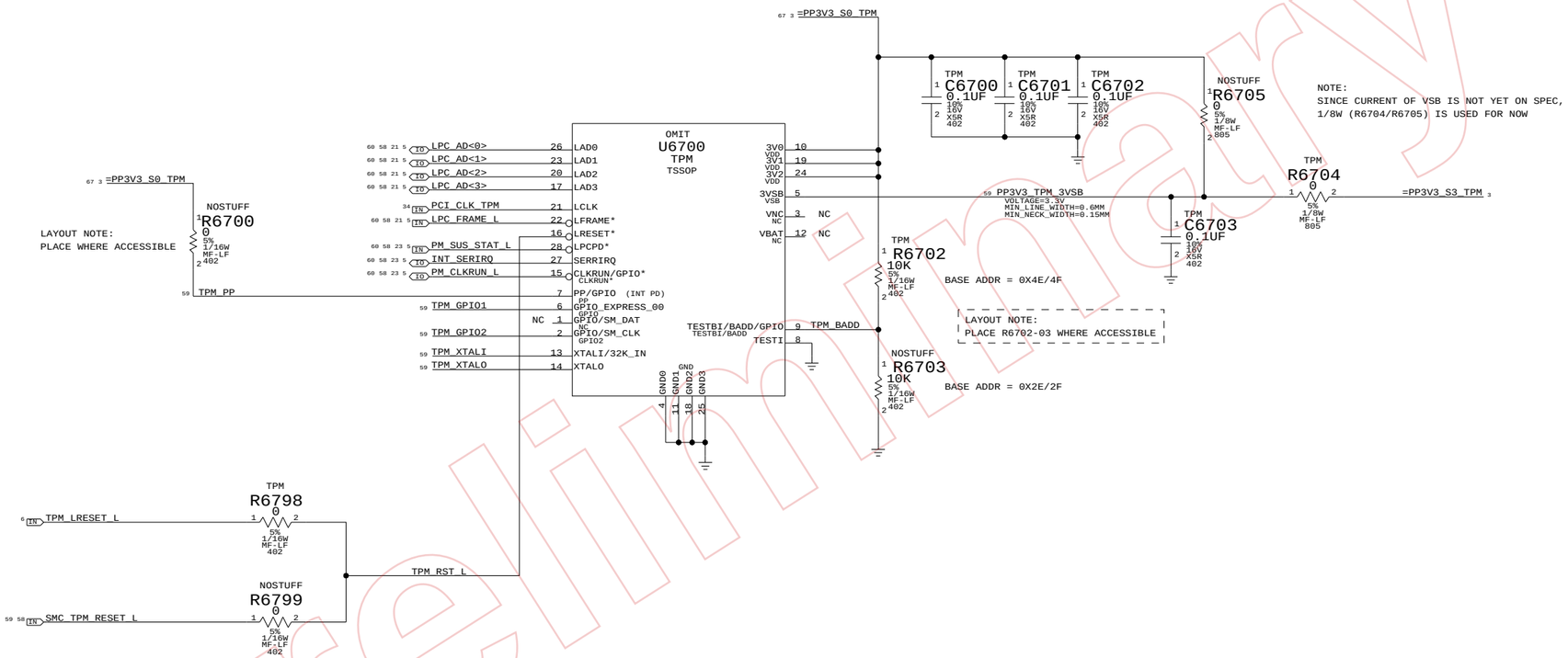

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TPM

SYNC_MASTER=M51_HENRY SYNC_DATE=08/04/2006

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D	051-7039	H
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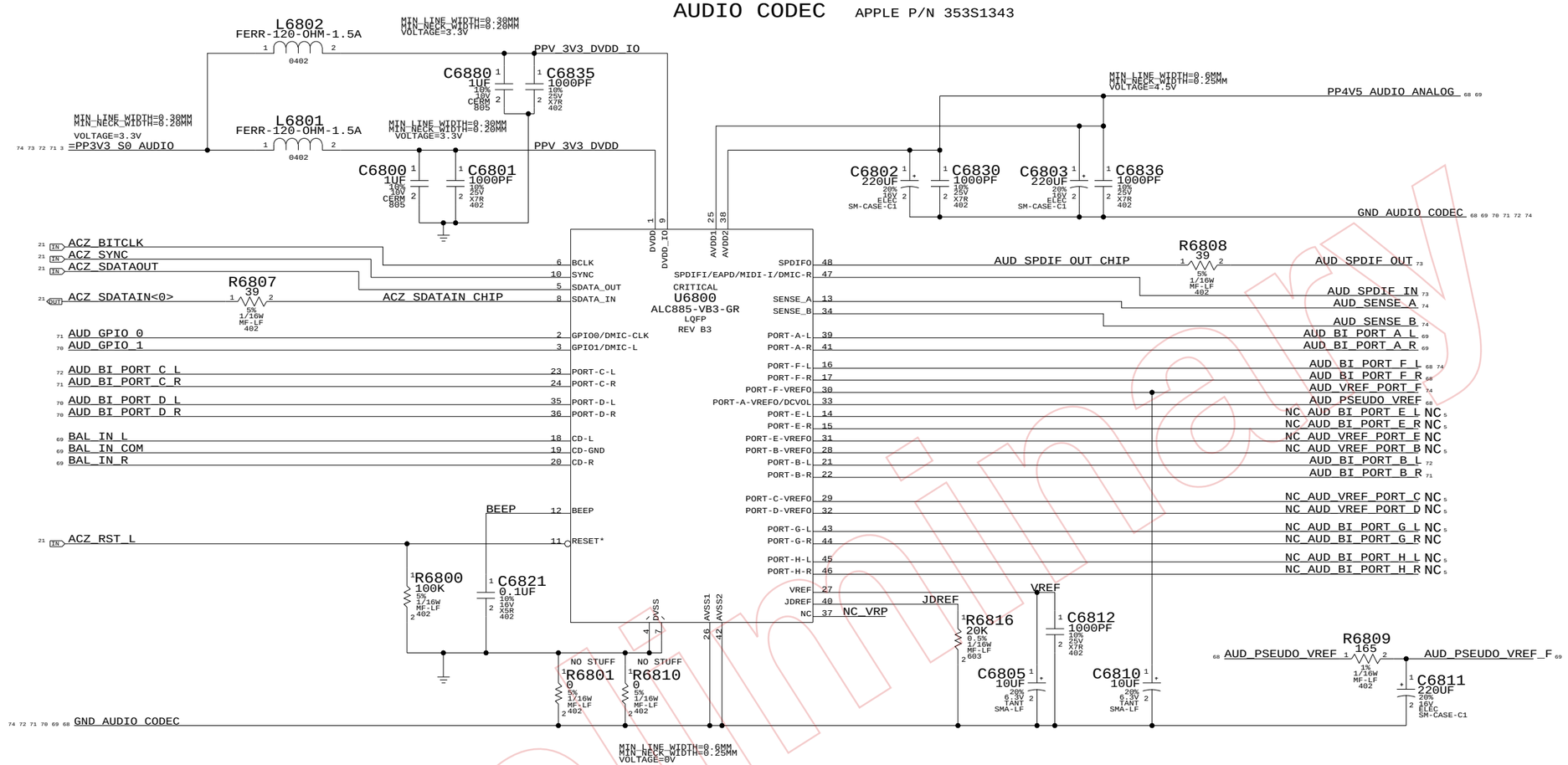
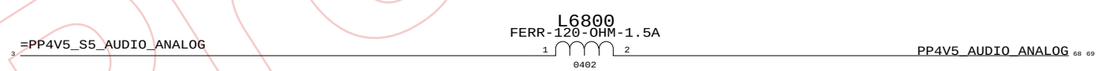
AUDIO CODEC

APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

MIC INPUT TO BOTH L&R



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AUDIO: CODEC	
SYNC_MASTER=AUDIO	SYNC_DATE=08/04/2006

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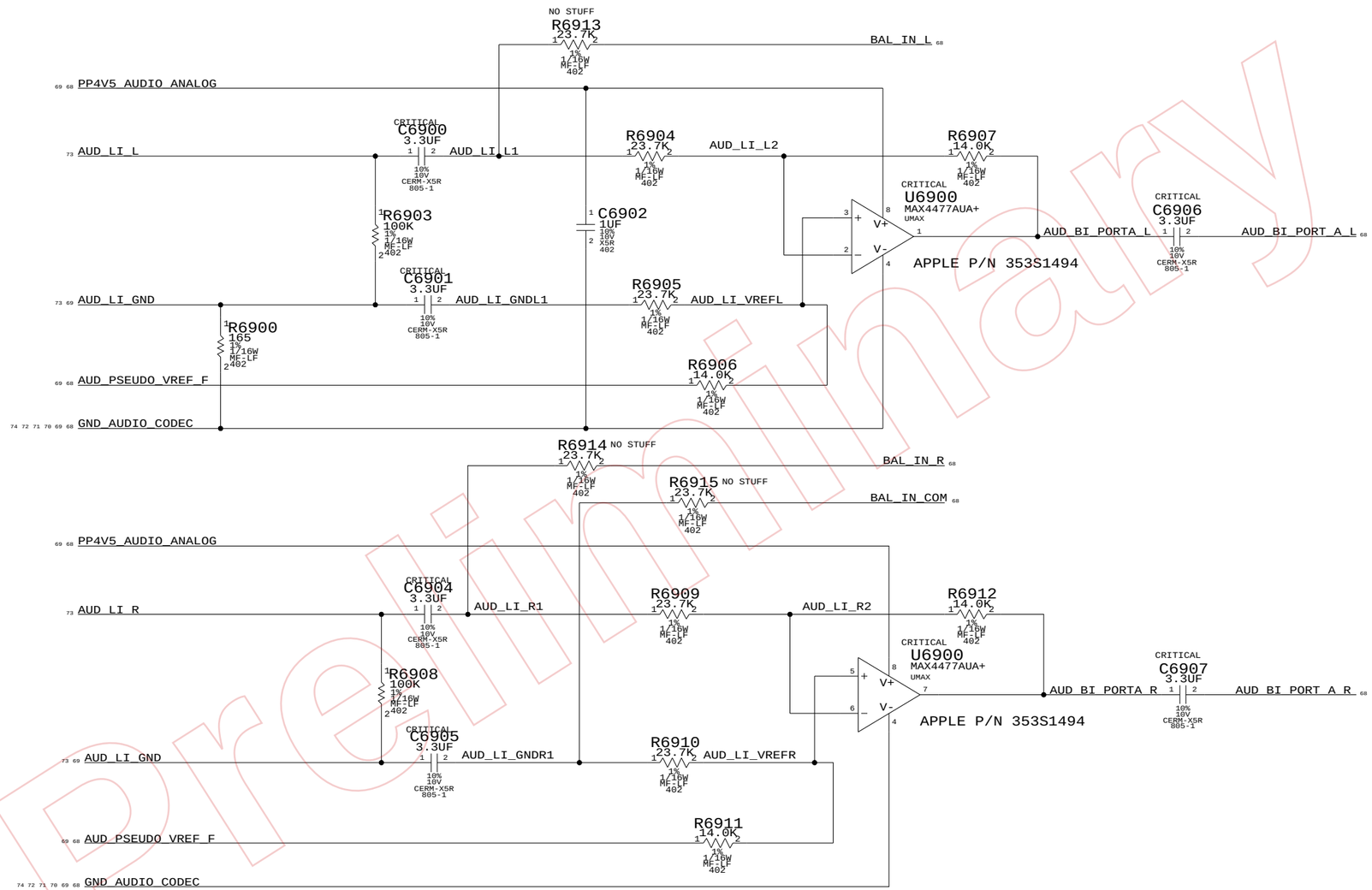
LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59



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AUDIO: LINE INPUT AMP

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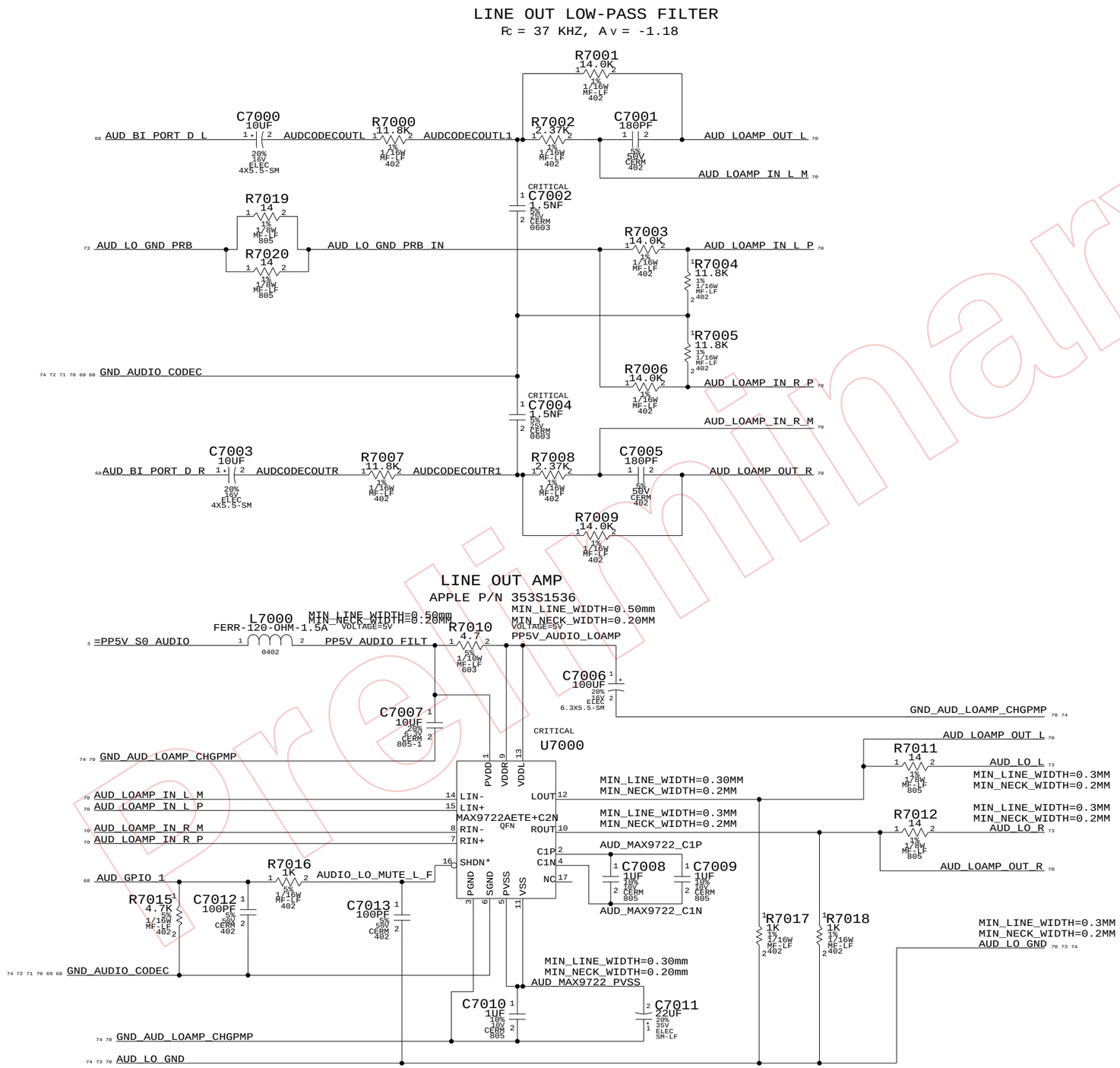
SCALE NONE	SHT 69 OF 97	



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AUDIO: COMBO OUT AMP

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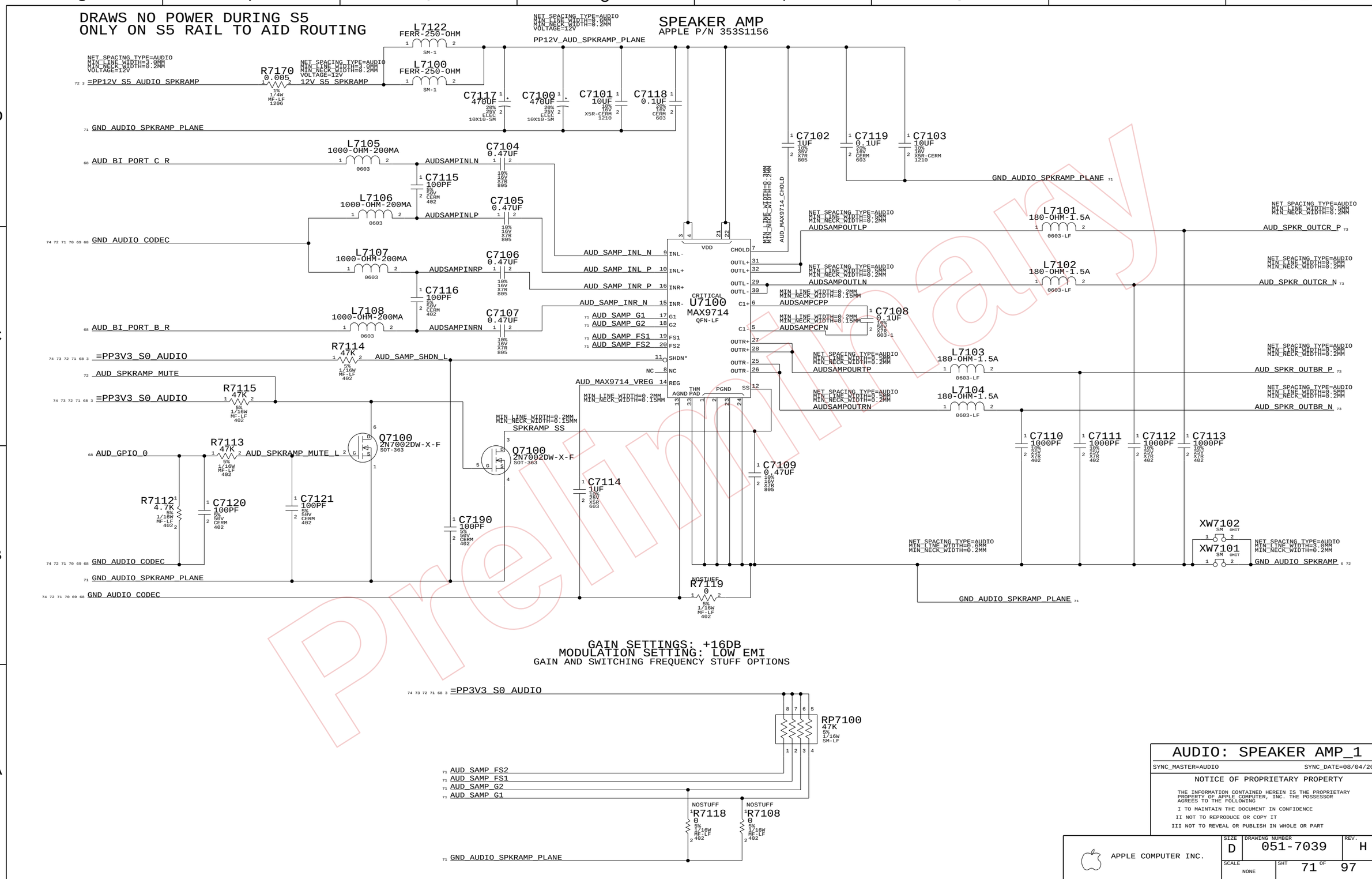
SCALE NONE	SHT 70 OF 97	



AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

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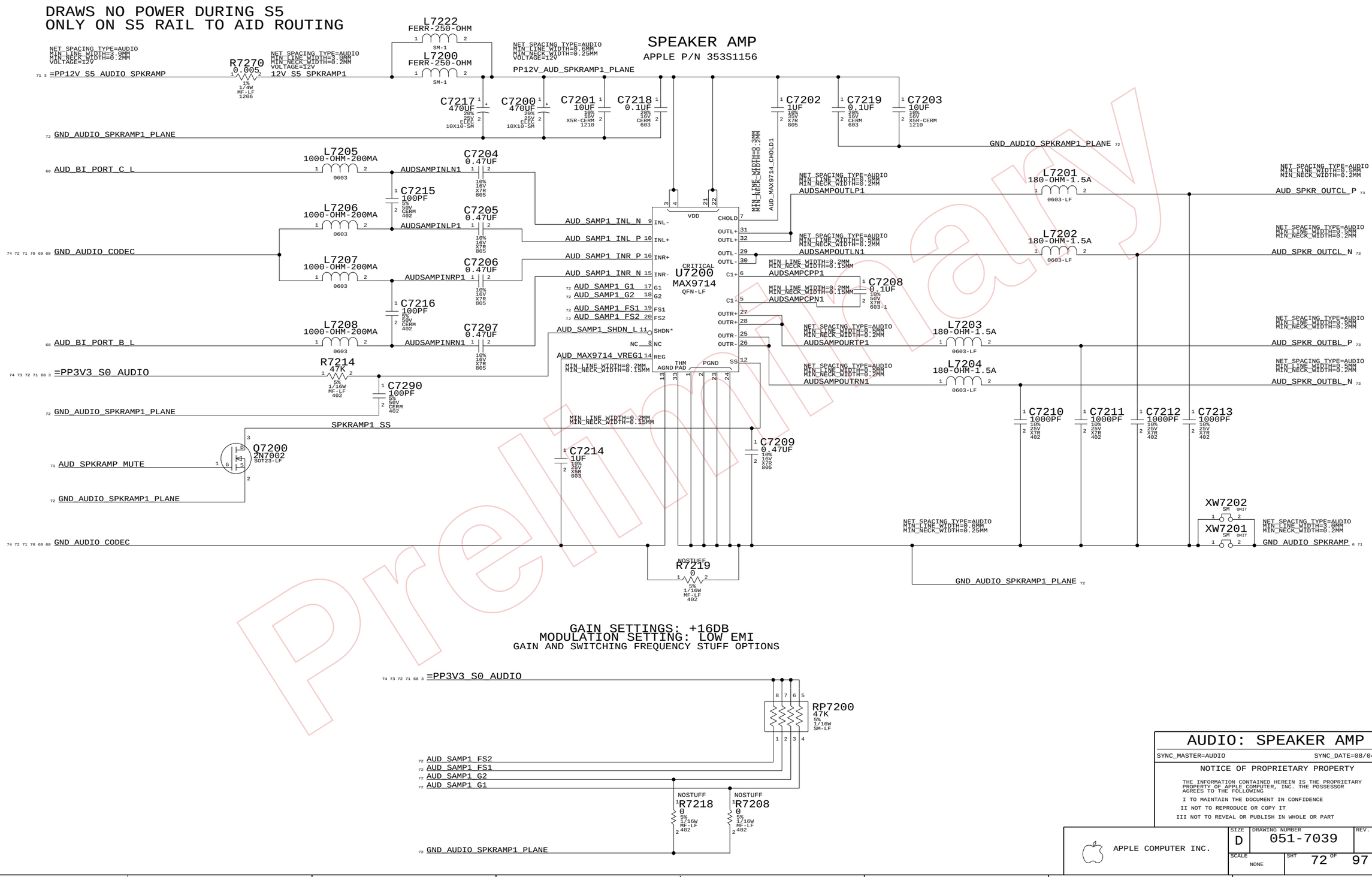

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

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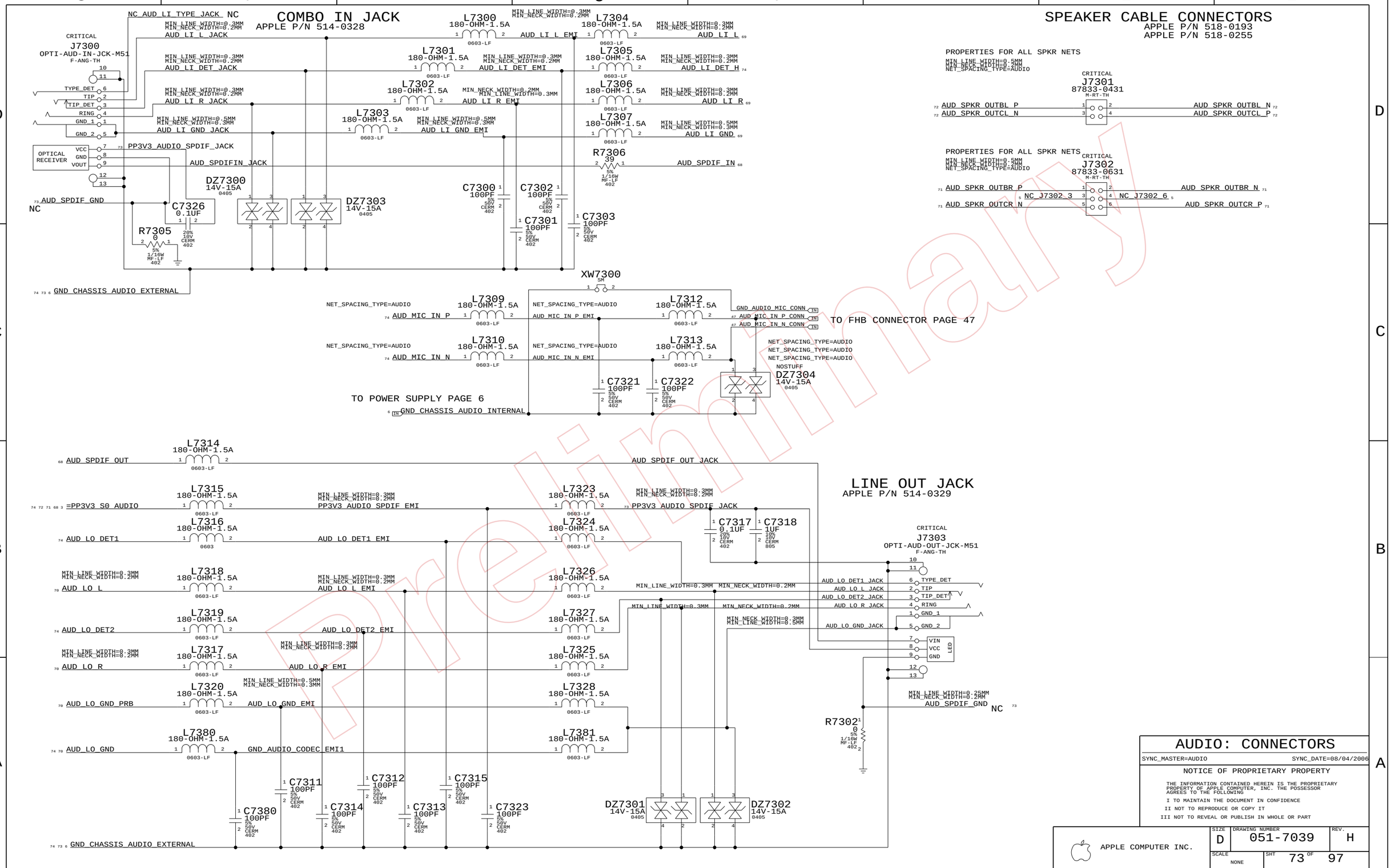

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AUDIO: CONNECTORS

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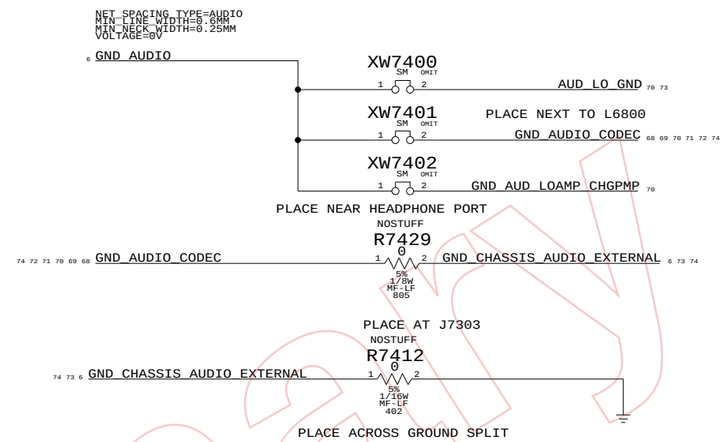
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14(D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18(B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A(C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN 0X16H		

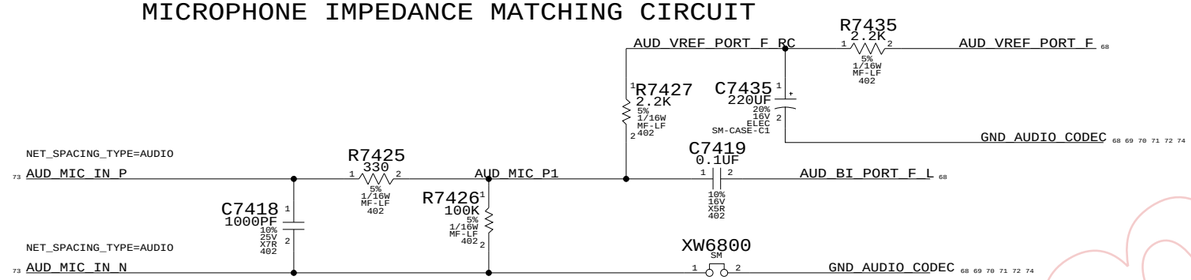
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19(F)	80%
LINE INPUT	0X08	0X23	0X15(A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

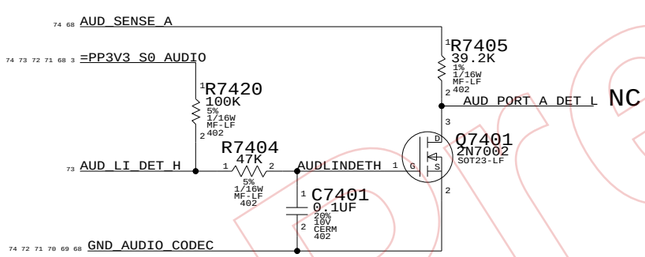
AUDIO GROUND RETURNS



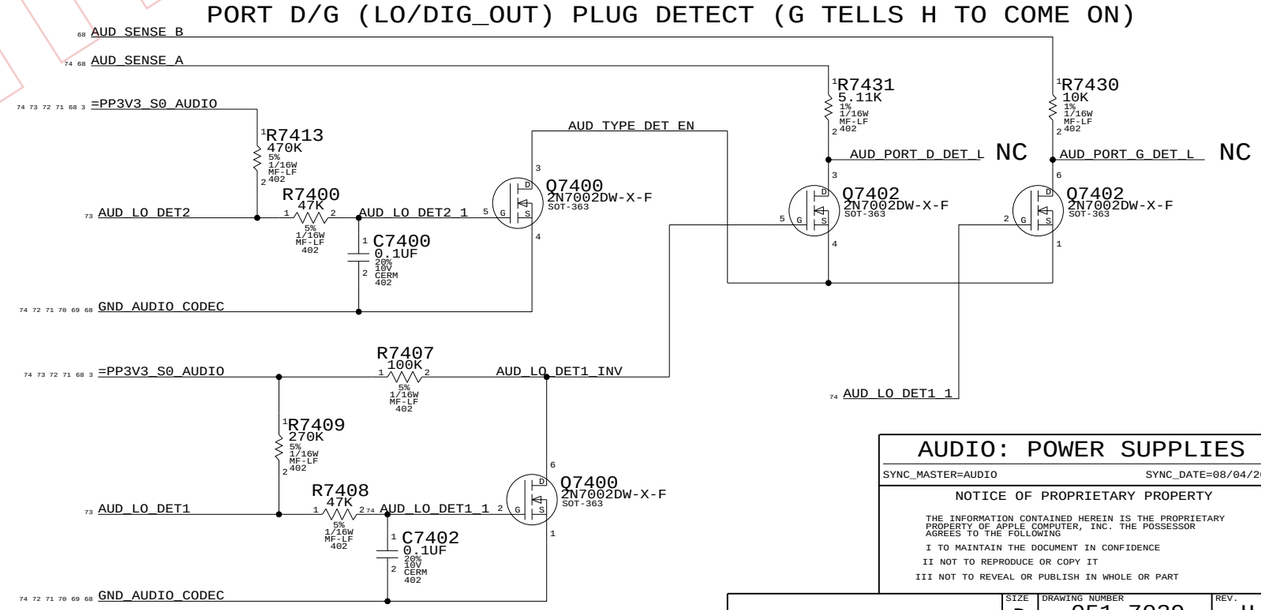
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=08/04/2006

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SCALE NONE	SHT 74 OF 97	

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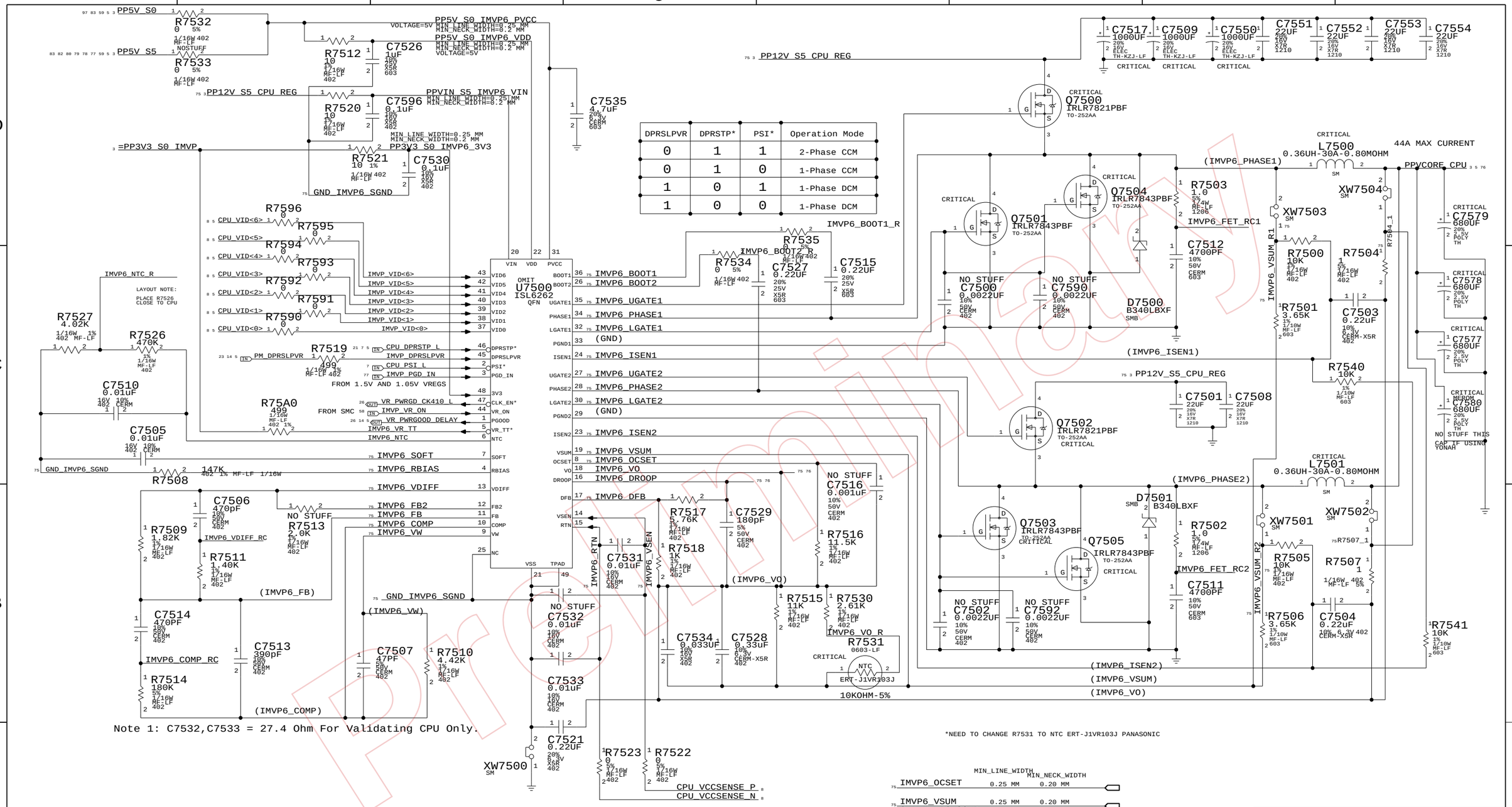

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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SCALE NONE SHT 75 OF 97

PROCESSOR VCORE SENSE

PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)

PPVCORE_CPU — CPU_PWR_SENSE R7612 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_VSENSE

CPU_PWR_SENSE C7612 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS

PROCESSOR VCORE CURRENT SENSE

(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

CPU_PWR_SENSE C7600 470PF 10% 50V CERM 402 — CPU_PWR_SENSE R7600 1M 1% 1/16W MF-LF 402 — CPU_ISENSE_OUT_R

IMVP6_VO — CPU_PWR_SENSE R7659 0 5% 1/16W MF-LF 402 — IMVP6_VO_R_OA

PP3V3_S0 — CPU_PWR_SENSE C7601 0.1UF CERM 20% 402 10V CRITICAL

CPU_PWR_SENSE R7605 40.2K 1% 1/16W MF-LF 402 — CPU_ISENSE_R_POS

CPU_PWR_SENSE U7600 LMV2011MF SOT23-5 — GND_CPU_ISENSE_OPAMP

IMVP6_DROOP — CPU_PWR_SENSE R7669 0 5% 1/16W MF-LF 402 — IMVP6_DROOP_R

CPU_PWR_SENSE R7606 40.2K 1% 1/16W MF-LF 402 — CPU_ISENSE_R_NEG

PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)

CPU_PWR_SENSE R7602 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_ISENSE

CPU_PWR_SENSE C7602 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS

MIN_LINE_WIDTH=0.20 MM

CPU_PWR_SENSE C7603 470PF 10% 50V CERM 402 — CPU_PWR_SENSE R7603 1M 1% 1/16W MF-LF 402

NOSTUFF R7604 0 5% 1/16W MF-LF 402

CPU_PWR_SENSE R7607 0 5% 1/16W MF-LF 402 — GND_NEXT_TO_SMC

CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

PP12V_S0_B — CPU_PWR_SENSE R7639 10K 5% 1/16W MF-LF 402 — CPU_PWR_SENSE Q7640 NTR4101P SOT-23

ISENSE_CAL_EN_L — MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.20 MM

CPU_PWR_SENSE R7641 10K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_L_R — CPU_PWR_SENSE Q7639 2N7002 SOT23-LF

ISENSE_CAL_EN — CPU_PWR_SENSE R7640 100K 5% 1/16W MF-LF 402

ISENSE_CAL_EN_LS12V — CPU_PWR_SENSE R7642 470K 5% 1/16W MF-LF 402

=PPVCORE_S0_CPU — CPU_PWR_SENSE R7643 1.00 1% 1/4W MF-LF 1206

CPUVCORE_ISENSE_CAL — MIN_LINE_WIDTH=0.50 mm, MIN_NECK_WIDTH=0.20 mm

CRITICAL Q7641 FDC796N SUPERSOT-6 CPU_PWR_SENSE

SYSTEM CURRENT SENSE

PP12V_S5_AC_DC — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

CRITICAL R7650 0.005 1% MF 2010 — SYS_PWR_SENSE — PP12V_S5

PCB:KEEP SHORTS NEXT TO U7602
PCB:PLACE D7650,R7652,C7650 BY SMC

SYS_PWR_SENSE CRITICAL U7602 ZXCT1010 SOT23-5 (VIN, NC, IOUT, LOAD, GND)

SCALE	COUNT
3.33333 A/V	.010753 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

OMIT XW7650 SM — SYSTEM_DCIN_SENSE — SYSTEM_SENSE_I_R

SYS_PWR_SENSE R7651 5.90K 1% 1/16W MF-LF 402

SYS_PWR_SENSE R7656 100 1% 1/16W MF-LF 402 — SYSTEM_SENSE_SET

SYS_PWR_SENSE R7652 4.53K 1% 1/16W MF-LF 402 — SMC_DCIN_ISENSE

PP3V3_S0 — NOSTUFF D7650 BAS16-75V-0.25A SOT23-LF → TO SMC

SYS_PWR_SENSE C7650 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS

1 MS TIME CONSTANT
SO SMC ADC SAMPLING
WORKS WELL.

PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)

SYSTEM VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)

PP12V_S5 — SYS_PWR_SENSE R7653 6.04K 1% 1/16W MF-LF 402 — SMC_SYSTEM_VSENSE_R1

SCALE	COUNT
4 V/V	.0129 V/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

SYS_PWR_SENSE R7655 4.53K 1% 1/16W MF-LF 402 — SMC_PBUS_VSENSE

PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)

SYS_PWR_SENSE R7654 2.0K 1% 1/16W MF-LF 402

SYS_PWR_SENSE C7651 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS

SMC PWRGD PULLUP

PP3V3_S5 — R7623 10K 1% 1/16W MF-LF 402

NOSTUFF R7620 0 5% 1/16W MF-LF 402

SYS_POWERFAIL_L — RSMRST_PWRGD

Preliminary

CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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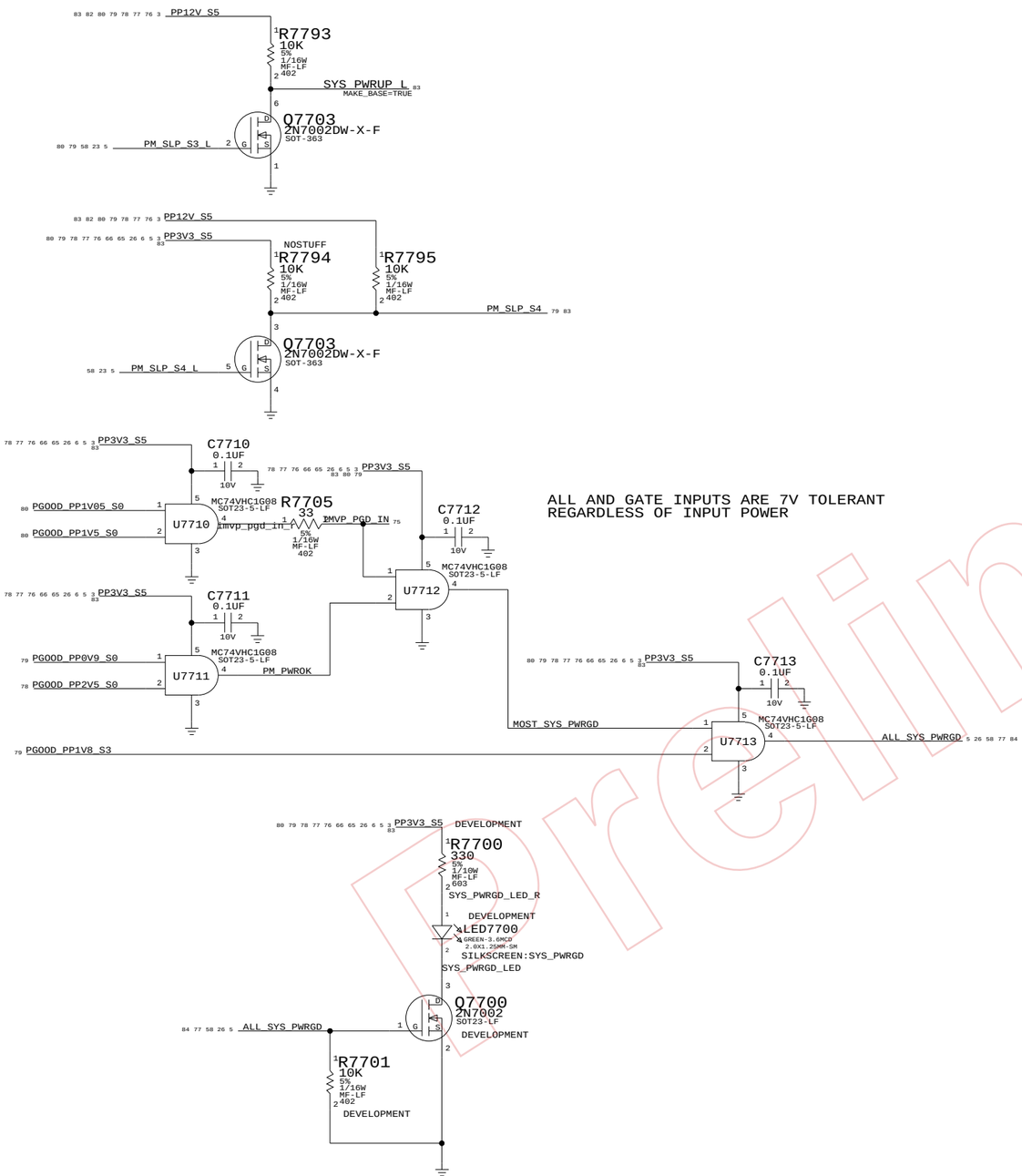
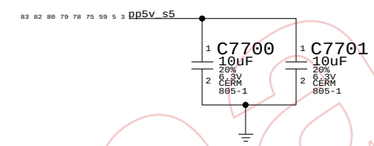
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 76 OF 97	



ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 on page 82



Preliminary

PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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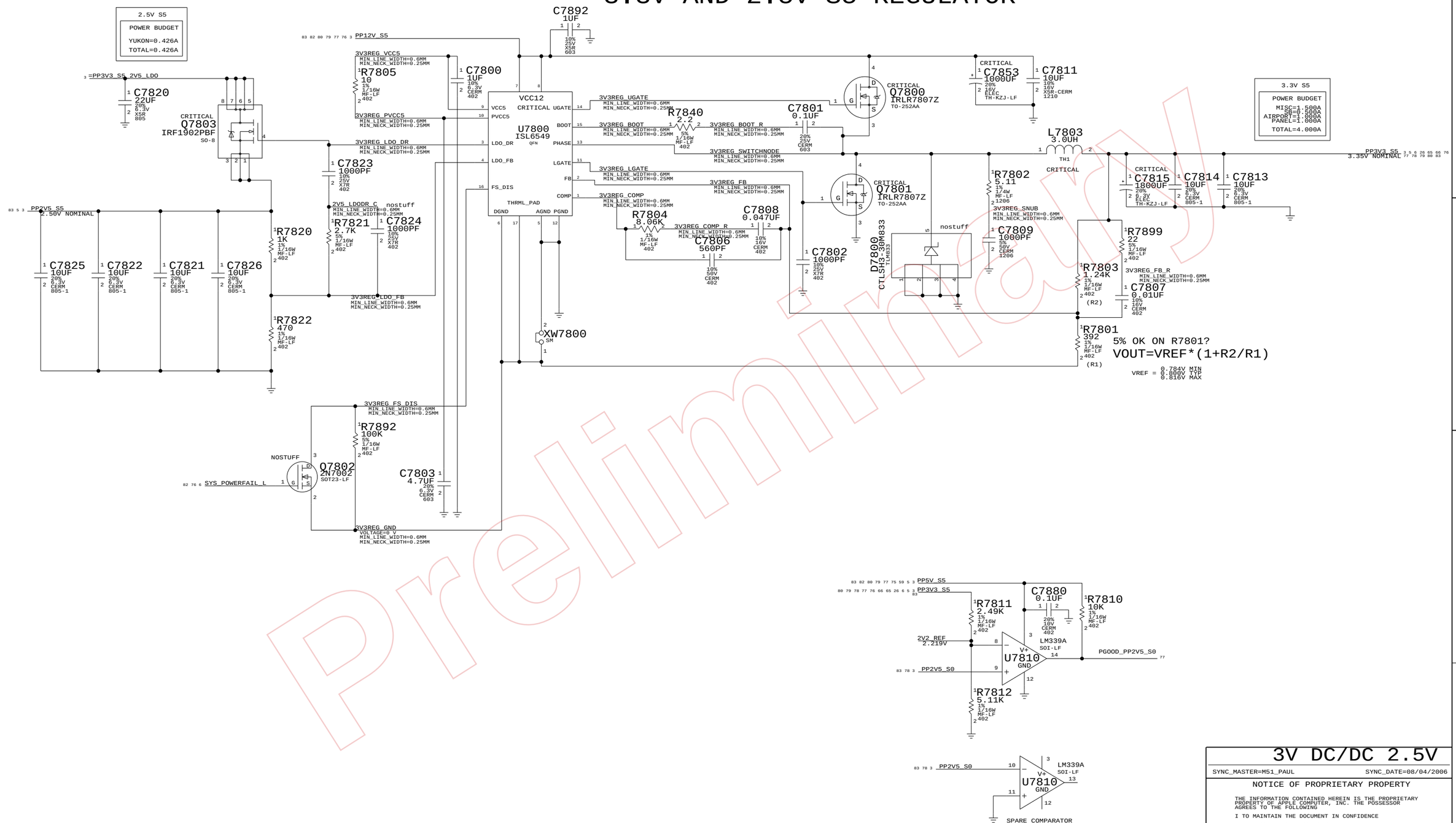
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 77 OF 97	

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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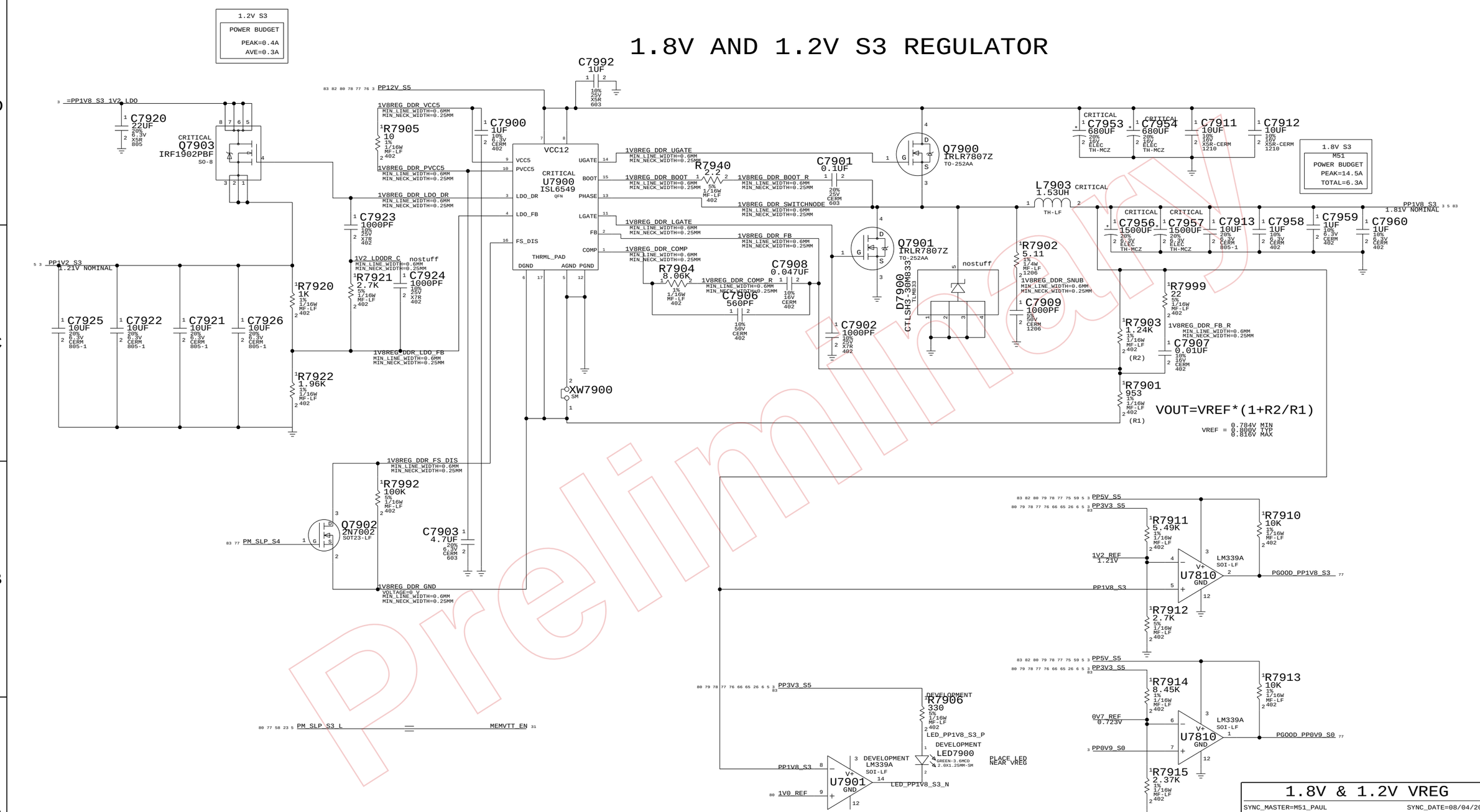
SIZE	DRAWING NUMBER	REV.
D	051-7039	H

SCALE NONE — SHT 78 OF 97

Preliminary

1.8V AND 1.2V S3 REGULATOR



1.8V & 1.2V VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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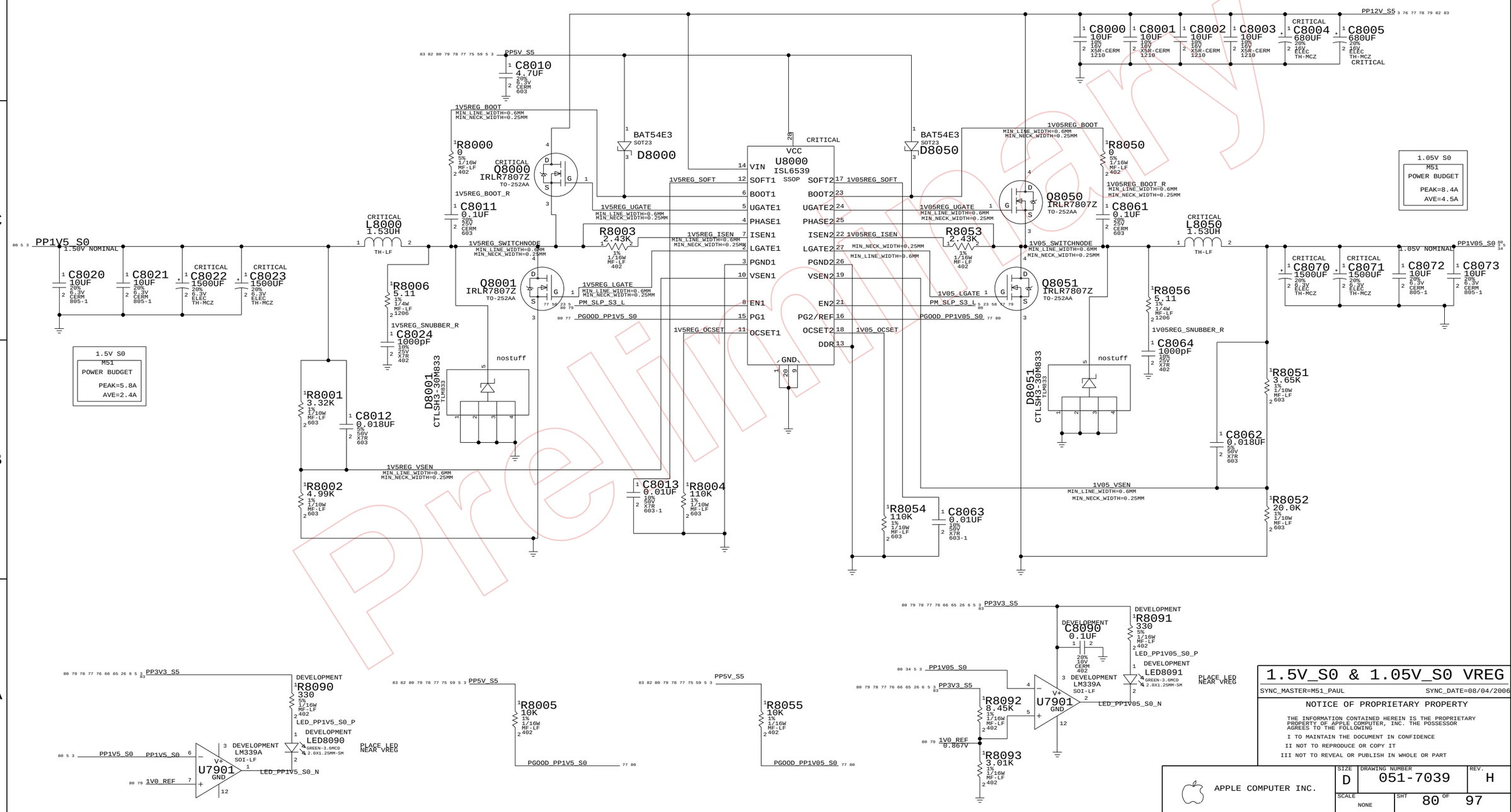
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 79 OF 97	

Preliminary

1.5V S0 AND 1.05V S0 RAILS



1.5V_S0 & 1.05V_S0 VREG

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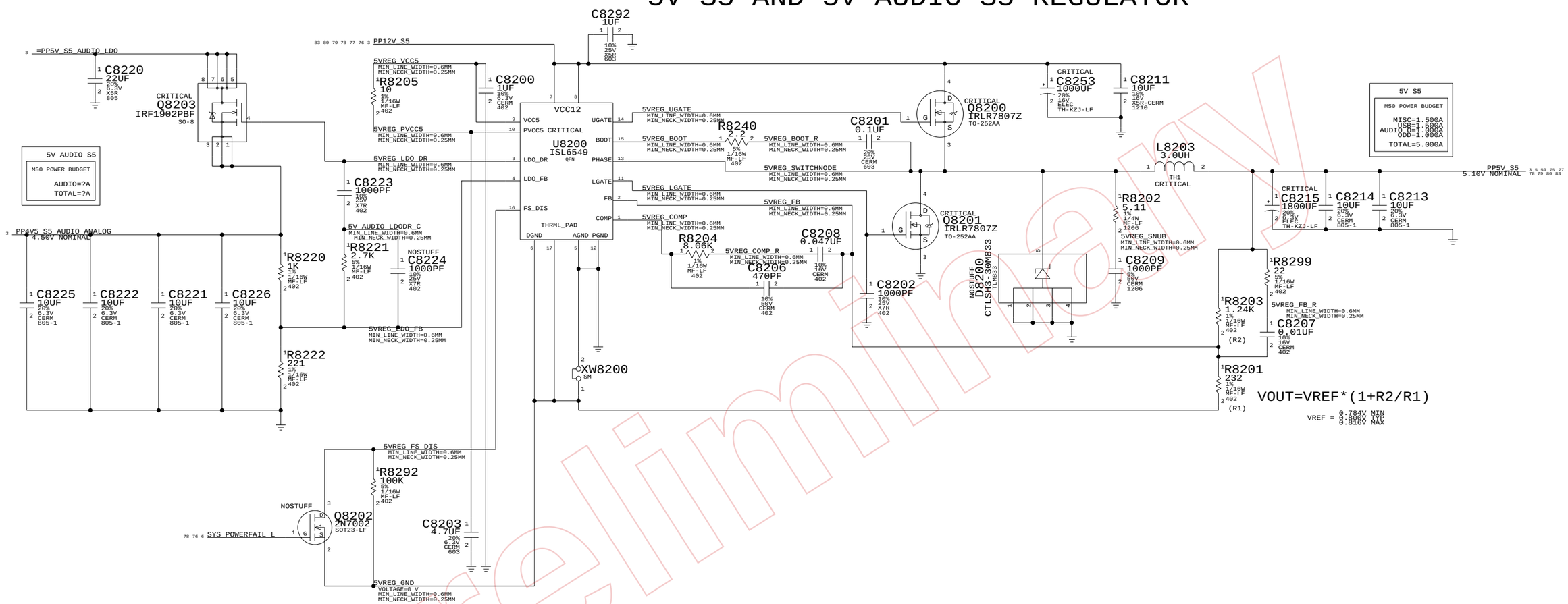
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 80 OF 97	

5V S5 AND 5V AUDIO S5 REGULATOR



Preliminary

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

SYNC_MASTER=M51_PAUL SYNC_DATE=08/04/2006

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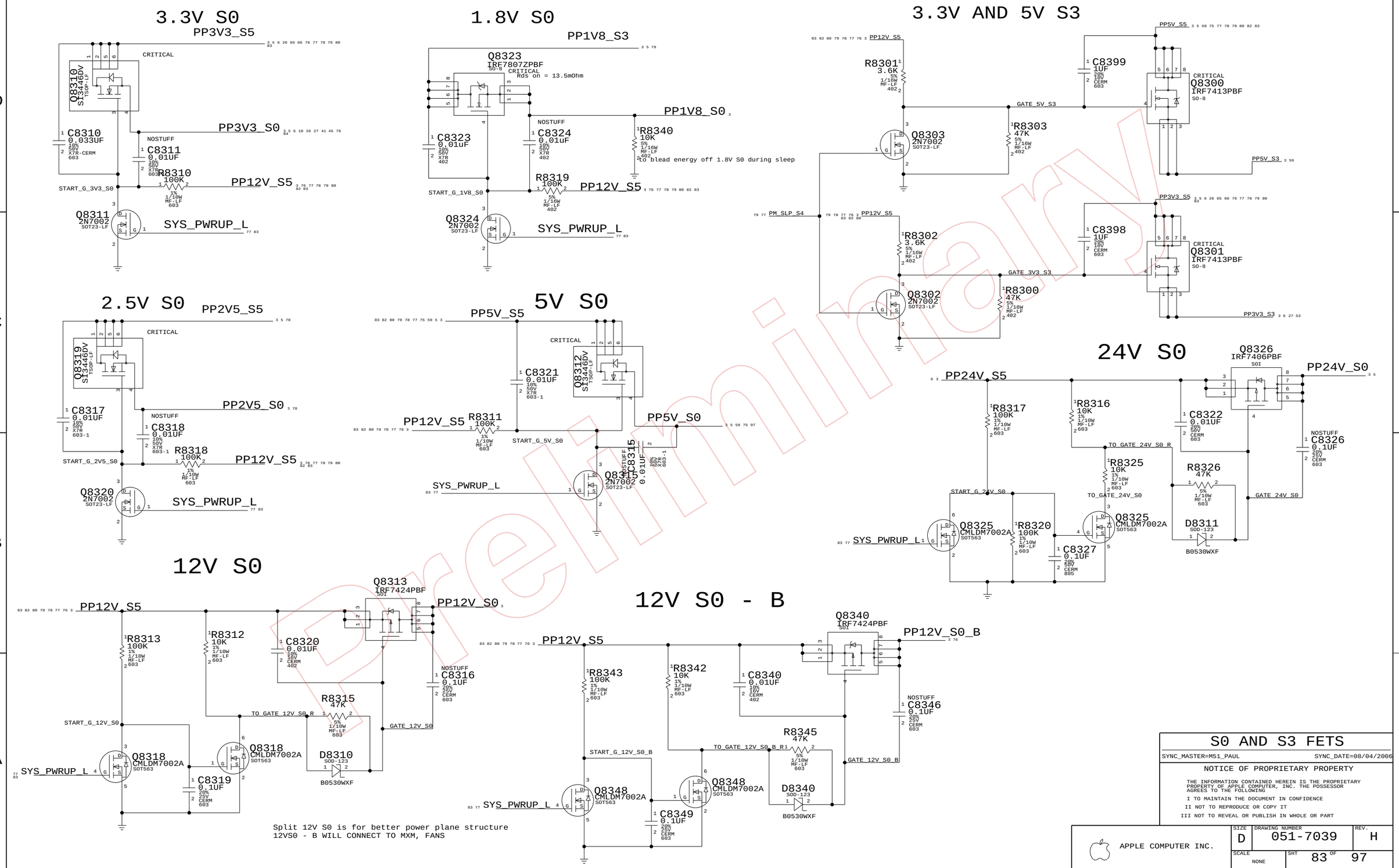
SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 82 OF 97	



Preliminary

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

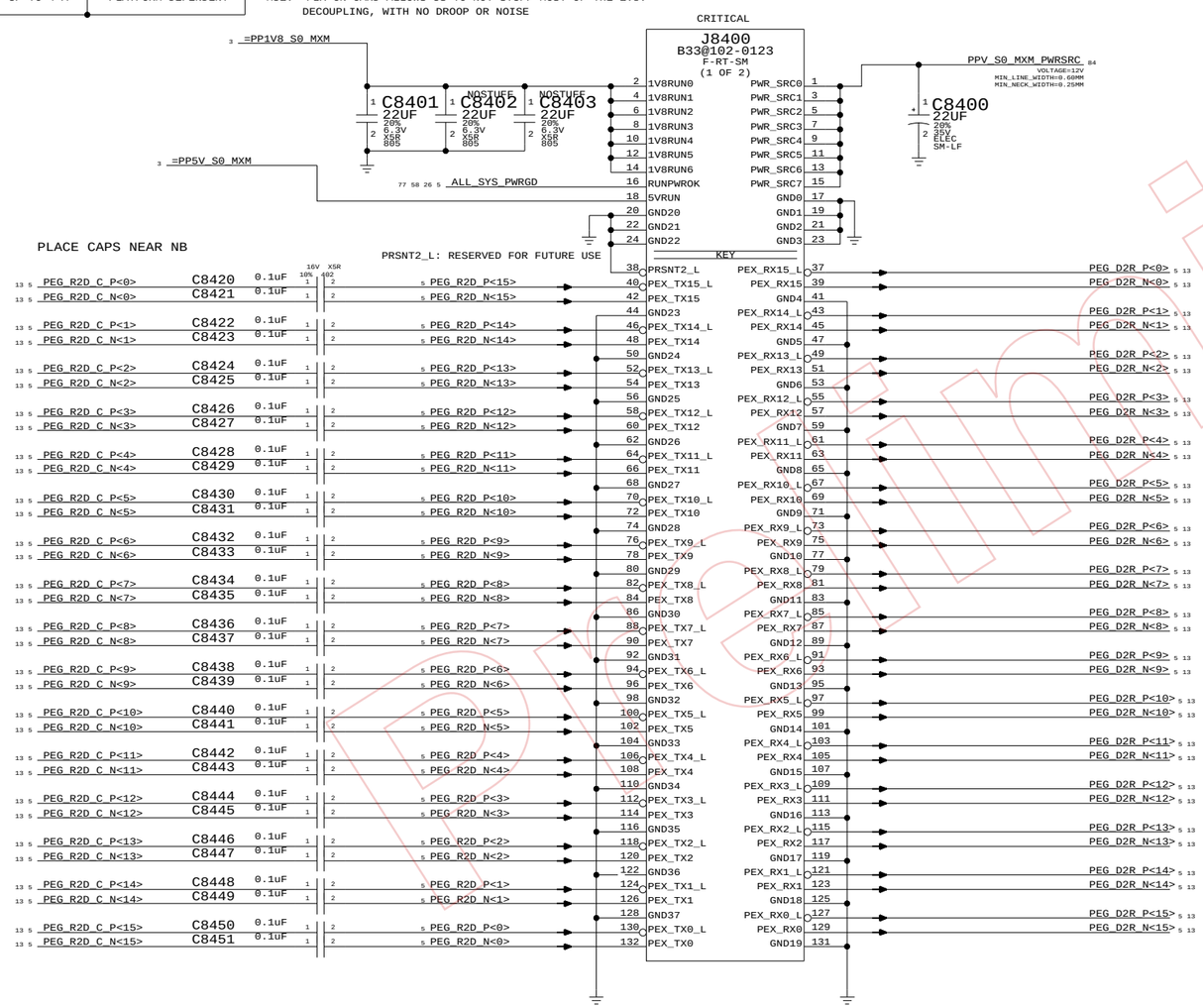
BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

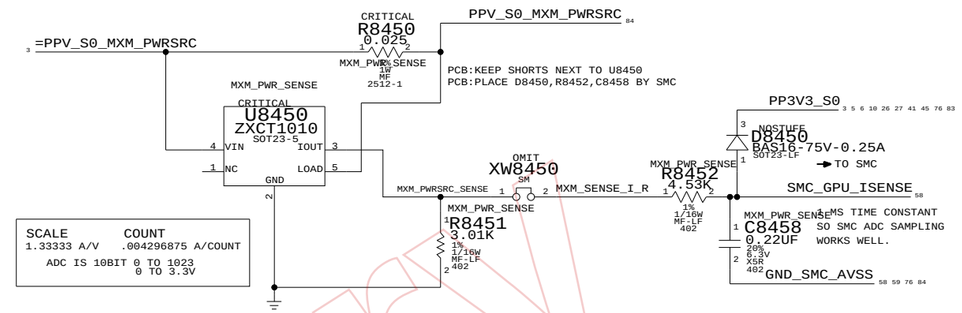
MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

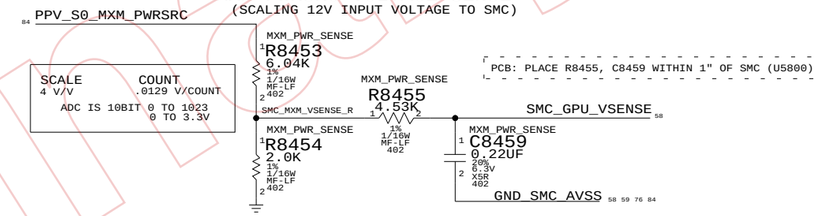
M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE



MXM PWRSRC (GPU CORE) CURRENT SENSE



MXM PWRSRC VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 84 OF 97	

Page Notes

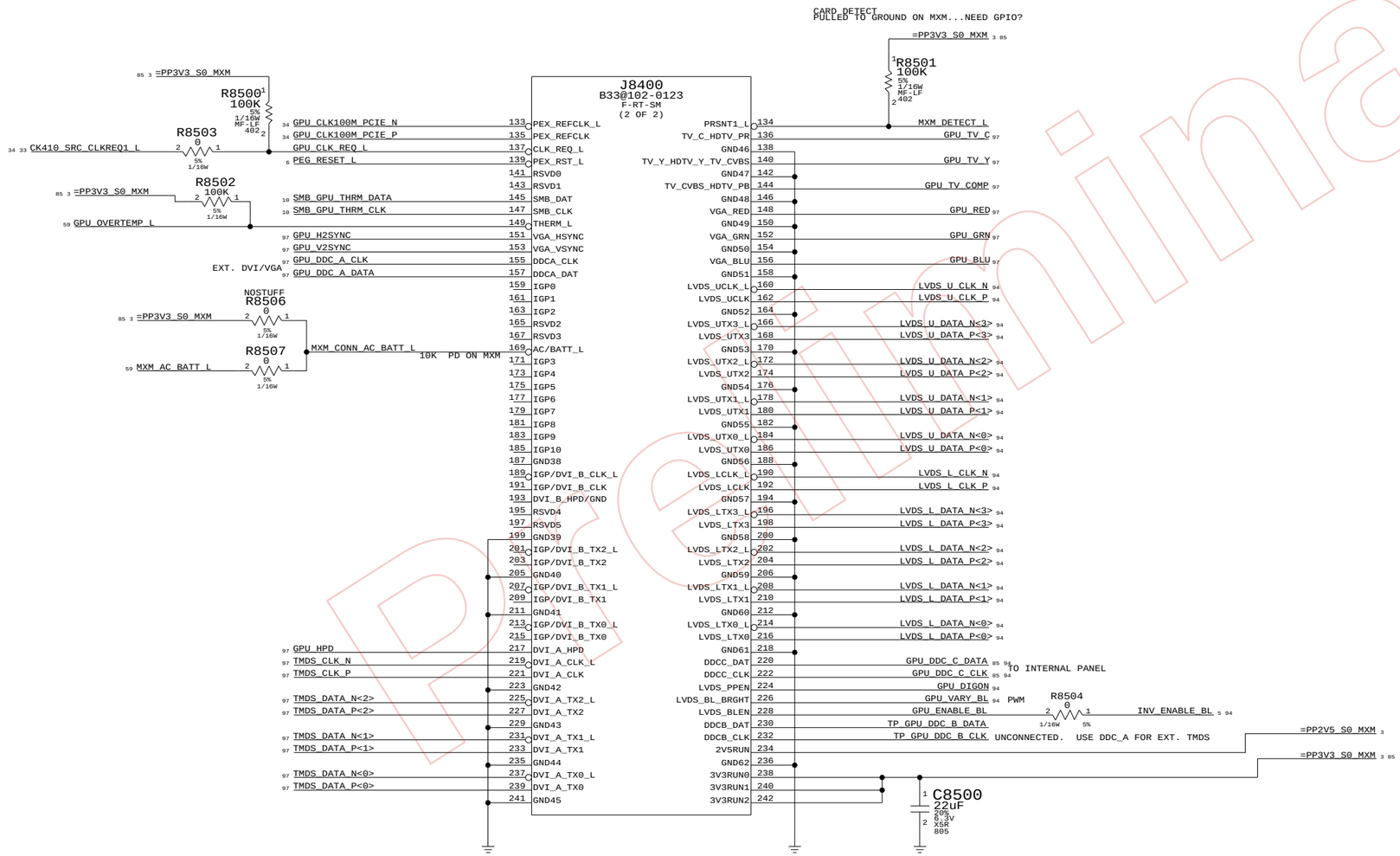
Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

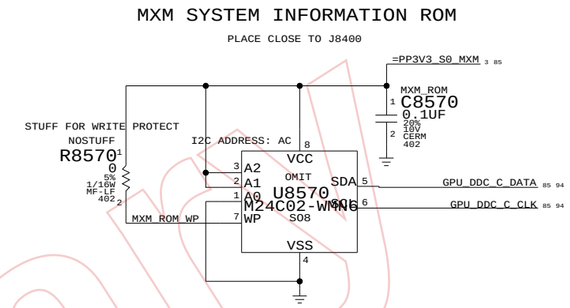
Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT





Preliminary

MXM I/O

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 85 OF 97	

Page Notes

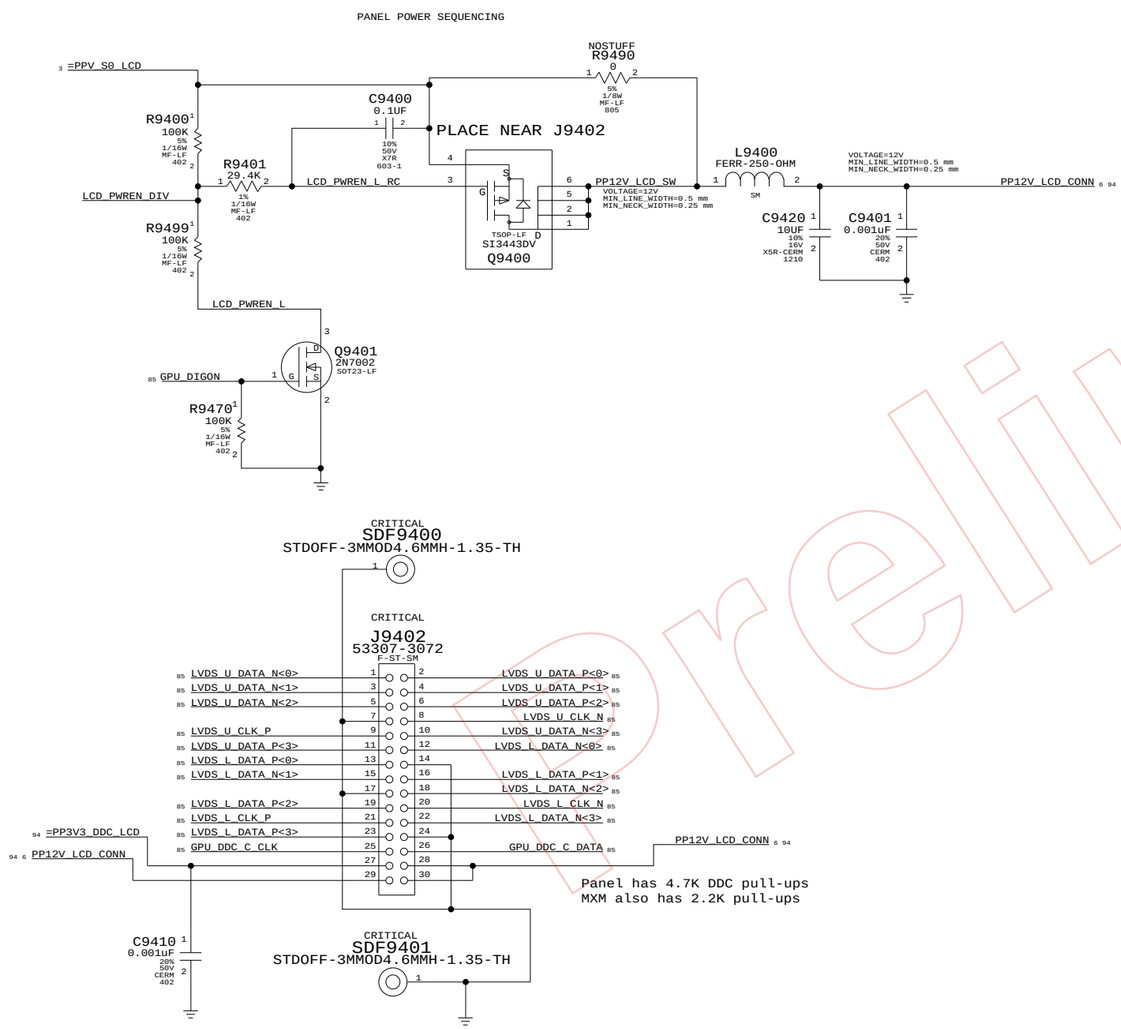
Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

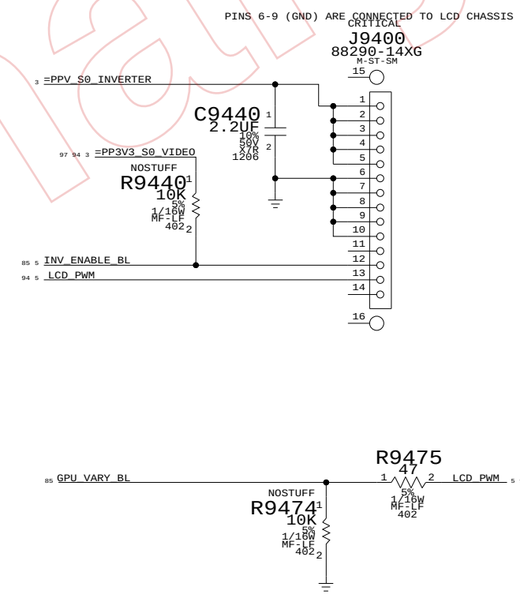
BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Preliminary

Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7039	H
SCALE NONE	SHT 94 OF 97	

DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

85 TMDS_DATA_N<0> — NOSTUFF R9700 0 — L9700 90-OHM CRITICAL — TMDS_CONN_DN<0> 97
85 TMDS_DATA_P<0> — NOSTUFF R9702 0 — TMDS_CONN_DP<0> 97
=PP3V3_S0_VIDEO 3 94 97 — NOSTUFF R9790 49.9 1% 1/16W MF-LF 402 — NOSTUFF R9791 49.9 1% 1/16W MF-LF 402

85 TMDS_DATA_N<1> — NOSTUFF R9703 0 — L9701 90-OHM CRITICAL — TMDS_CONN_DN<1> 97
85 TMDS_DATA_P<1> — NOSTUFF R9705 0 — TMDS_CONN_DP<1> 97
=PP3V3_S0_VIDEO 3 94 97 — NOSTUFF R9792 49.9 1% 1/16W MF-LF 402 — NOSTUFF R9793 49.9 1% 1/16W MF-LF 402

85 TMDS_DATA_N<2> — NOSTUFF R9704 0 — L9702 90-OHM CRITICAL — TMDS_CONN_DN<2> 97
85 TMDS_DATA_P<2> — NOSTUFF R9709 0 — TMDS_CONN_DP<2> 97
=PP3V3_S0_VIDEO 3 94 97 — NOSTUFF R9794 49.9 1% 1/16W MF-LF 402 — NOSTUFF R9795 49.9 1% 1/16W MF-LF 402

85 TMDS_CLK_N — NOSTUFF R9708 0 — L9703 90-OHM CRITICAL — TMDS_CONN_CLKN 97
TMDS_CONN_CLKP 97
85 TMDS_CLK_P — NOSTUFF R9715 0

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

83 75 59 5 3 PP5V_S0 — D9710 SOD-123 B0530WXF — PP5V_S0_DDC_DIODE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC 97 (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL
J9710 MINI-DVI-M51 F-ST-SM

97 DVI_HPD_UF — 25
17
97 DVI_DDC_CLK_UF — 26
97 DVI_DDC_DATA_UF — 18
27
19
28
97 VGA_BLU — 20
97 VGA_HSYNC — 29
30
97 VGA_GRN — 22
97 VGA_VSYNC — 31
32
97 VGA_RED — 24
33 34

1 — TMDS_CONN_DP<2> 97
9
2 — TMDS_CONN_DN<2> 97
10
3 — TMDS_CONN_DP<1> 97
11
4 — TMDS_CONN_DN<1> 97
12
5 — TMDS_CONN_DP<0> 97
13
6 — TMDS_CONN_DN<0> 97
14
7 — TMDS_CONN_CLKP 97
15
8 — TMDS_CONN_CLKN 97
16

DVI_CHASSIS 33
C9720 0.1UF 10% 16V X5R 402 — C9721 0.1UF 10% 16V X5R 402
GND_CHASSIS_DVI 6

PLACE CLOSE TO MINI-DVI CONNECTOR 3V LEVEL SHIFTERS

97 PP5V_S0_DDC
97 =PP3V3_S0_VIDEO

R9710 4.7K 5% 1/10W MF-LF 402 — R9712 4.7K 5% 1/10W MF-LF 402
97 DVI_DDC_CLK_UF — R9711 100 5% 1/10W MF-LF 402 — DVI_DDC_CLK — Q9711 2N7002DW-X-F SOT-363 — R9720 10K 5% 1/10W MF-LF 402 — GPU_DDC_A_CLK 85
C9711 100pF 5% 50V CERM 402
97 DVI_DDC_DATA_UF — R9713 100 5% 1/10W MF-LF 402 — DVI_DDC_DATA — Q9711 2N7002DW-X-F SOT-363 — R9721 10K 5% 1/10W MF-LF 402 — GPU_DDC_A_DATA 85
C9713 100pF 5% 50V CERM 402
97 DVI_HPD_UF — R9714 0 5% 1/10W MF-LF 402 — GPU_HPD 85
C9710 0.01uF 20% 50V CERM 603 — C9714 100pF 5% 50V CERM 402
NOSTUFF R9722 100K 5% 1/10W MF-LF 402 — NOSTUFF D9700 CASE425 MMSZ4681XXG

Note: this clamp is supposed to be on the MXM card

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

=PP3V3_S0_VIDEO 3 94 97
C9730 0.1UF 20% 10V CERM 402 — C9731 10uF 20% 6.3V CERM 805-1

U9730 SOP TS3V330 CRITICAL
VCC 16
85 GPU_TV_C — S1A 2 — DA 4 — VIDEO_MUX_RED
85 GPU_RED — S2A 3
85 GPU_TV_Y — S1B 5 — DB 7 — VIDEO_MUX_GRN
85 GPU_GRN — S2B 6
85 GPU_TV_COMP — S1C 11 — DC 9 — VIDEO_MUX_BLU
85 GPU_BLU — S2C 10
NC — S1D 14 — DD 12 — NC
NC — S2D 13 — IN 1 — SB_CRT_TVOUT_MUX 22
EN_L 15
GND 8

R9740 150 1% 1/16W MF-LF 402 — NOSTUFF C9743 10PF 5% 50V CERM 402 — L9740 27NH-200MA 0402 — C9740 10PF 5% 50V CERM 402 — VGA_BLU 97
R9741 150 1% 1/16W MF-LF 402 — NOSTUFF C9744 10PF 5% 50V CERM 402 — L9741 27NH-200MA 0402 — C9741 10PF 5% 50V CERM 402 — VGA_GRN 97
R9742 150 1% 1/16W MF-LF 402 — NOSTUFF C9745 10PF 5% 50V CERM 402 — L9742 27NH-200MA 0402 — C9742 10PF 5% 50V CERM 402 — VGA_RED 97

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR

97 94 3 =PP3V3_S0_VIDEO
C9760 0.1UF 20% 10V CERM 402

85 GPU_V2SYNC — U9760 74LC125 125 TSSOP — GPU_VSYNC_BUF 1 — R9760 33 5% 1/10W MF-LF 402 — VGA_VSYNC_R — L9760 27NH-200MA 0402 — VGA_VSYNC 97

85 GPU_H2SYNC — U9760 74LC125 125 TSSOP — GPU_HSYNC_BUF 1 — R9761 33 5% 1/10W MF-LF 402 — VGA_HSYNC_R — L9761 27NH-200MA 0402 — VGA_HSYNC 97
C9762 10PF 5% 50V CERM 402 — C9763 10PF 5% 50V CERM 402

DISABLE UNUSED BUFFERS

U9760 74LC125 125 TSSOP — U9760 74LC125 125 TSSOP
97 94 3 =PP3V3_S0_VIDEO

Preliminary

External Display Conns	
SYNC_MASTER=M51_DAVE	SYNC_DATE=(MASTER)

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